

AR7643

TOUCH PANEL CONTROLLER

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HEADQUARTER

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May 27, 2001 Preliminary



FEATURES

- SERIAL INTERFACE
- 4-WIRE TOUCH PANEL INTERFACE
- EMBEDDED TOUCH PANEL DRIVERS
- 2.7V TO 5.5V SUPPLY VOLTAGE
- 12-BIT ANALOG TO DIGITAL CONVERTER
- PROGRAMMABLE 8- OR 12-BIT RESOLUTION
- UP TO 125KHz CONVERSION RATE
- 2 AUXILIARY ANALOG INPUTS
- FULL POWER-DOWN CONTROL
- 16 PIN SSOP PACKAGE

APPLICATIONS

- TOUCH PANELS
- PERSONAL DIGITAL ASSISTANTS (PDA)
- POINT-OF-SALES TERMINALS
- PAGES
- HIGH SPEED DATA ACQUISTION
- PORTABLE INSTRUMENTS
- LOW POWER INSTRUMENTS

Ordering Information

PART	PART TEMP. RANGE PACK	
AR7643	-40°C to +85°C	SSOP-16

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DESCRIPTION

The AR7643 Touch Panel Controller IC is a 12-bit analog-to-digital (ADC) converter with SPI serial interface and low on-resistance drivers for 4-wire resistive touch panels.

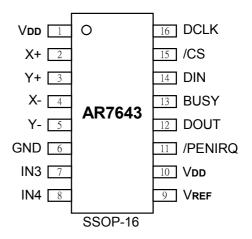
The AR7643 is a highly integrated controller for portable applications with 4-wire resistive touch panel such as, PDA, portable instruments, cellular phone, etc.

The AR7643 consumes only $800\mu W$ at a 125kHz sample rate and a 2.7V supply and consumes only 0.3 μW at shutdown mode. The AR7643 is guaranteed down to 2.7V supply.

The AR7643 is provided in a very small 16-lead SSOP package and is guaranteed over the temperature range.

Pin Configuration

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Absolute Maximum Rating

V _{DD} to GND	0.3V to +6V
Analog Input to GND	0.3V to V _{DD} +0.3V
Digital Input to GND	0.3V to V_{DD} +0.3V
Operating Temperature Range	40°C to +85°C
Maximum Junction Temperature	+150°C
Storage Temperature Range	60°C to +150°C
Lead Temperature (Soldering, 10s)	+300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

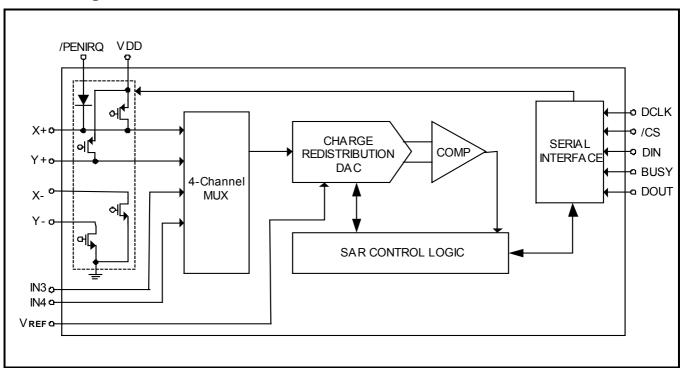
Electrostatic Discharge Sensitivity

This integrated circuit can be damaged by ESD. ARTi recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure.

Pin Description

Pin	Name	Description
1	V_{DD}	Power Supply, 2.7V to 5.5V.
2	X+	X+ Input; ADC Input Channel 1.
3	Y+	Y+ Input; ADC Input Channel 2.
4	X-	X- Input.
5	Y-	Y- Input.
6	GND	Ground.
7	IN3	Auxiliary Input 1; ADC Input Channel 3.
8	IN4	Auxiliary Input 2; ADC Input Channel 4.
9	V_{REF}	Reference Voltage Input.
10	V_{DD}	Power Supply, 2.7V to 5.5V.
11	/PENIRQ	Pen Interrupt. Requires 10K Ω to 100K Ω
		external pull-up resistor.
12	DOUT	Serial Data Output. This output pin is high
		impedance when /CS is high.
13	BUSY	Busy Output. This output pin is high
		impedance when /CS is high.
14	DIN	Serial Data Input.
15	/CS	Chip Select Input. This input is active low.
16	DCLK	External Clock Input.

Block Diagram



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ELECTRICAL SPECIFICATIONS

 $(T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}, V_{DD} = +2.7\text{V}, V_{REF} = +2.7\text{V}, f_{Sample} = 125\text{KHz}, f_{CLK} = 24 \cdot f_{Sample}, 12\text{-bit mode}, Digital Inputs = GND or +V_{DD}.$ Typical values are at $T_A = +25^{\circ}\text{C}$, unless otherwise noted.)

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Power Supply Requirements V _{DD} Nominal Supply Current Power Dissipation	Specified Performance Shut Down Mode	2.7	300 800	3.6	V μA μA μW
System Performance Resolution INL DNL Gain Error Offset Error			12 +/-2 +/-1 +/-4 +/-6		Bits LSB LSB LSB LSB
Digital Input/Output Logic Family VOH VOL VIH VIL /PENIRQ VOL	CMOS 100KΩ Pull-Up	V _{DD} ⋅ 0.8 V _{DD} ⋅ 0.7 -0.3	0. 6	0.4 V _{DD} + 0.3 0.8	V V V
Analog Input Input Span Input Range Capacitance		0 -0.2	25	V _{REF} V _{DD} + 0.2	V PF
Reference Input Range Input Current	Specified Performance	1	15	V_{DD}	V µA
X / Y Switches X+, Y+ X-, Y-	Switch On-Resistance Switch On-Resistance		5 5		Ω
Temperature Range Operating Temperature Range	Specified Performance	-40		+85	°C



Timing Specifications: $(T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}, \ V_{DD} \ge +2.7\text{V}, \ C_{LOAD} = 50\text{pF}. \ Typical values are at } T_A = +25^{\circ}\text{C}, \ unless otherwise noted.)$

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
T _{ACQ}	ADC acquisition time	500			ns
T _{CON}	ADC conversion time	6.5			μs
T _{CSF}	/CS falling to first DCLK rising	100			ns
T _{CSR}	/CS rising to DCLK ignored	0			ns
T _{DOF}	/CS falling to DOUT enable			200	ns
T _{DOR}	/CS rising to DOUT disable			200	ns
T _{BSF}	/CS falling to BUSY enable			200	ns
T _{BSR}	/CS rising to BUSY disable			200	ns
Тскн	DCLK High Period	200			ns
T _{CKL}	DCLK LOW Period	200			ns
T _{DIS}	DIN valid before DCLK rising	100			ns
T _{DIH}	DIN hold time after DCLK going high	15			ns
T _{DO}	DCLK falling to DOUT valid			200	ns
T _{BO}	DCLK falling to BUSY rising			200	ns

Timing Diagram:

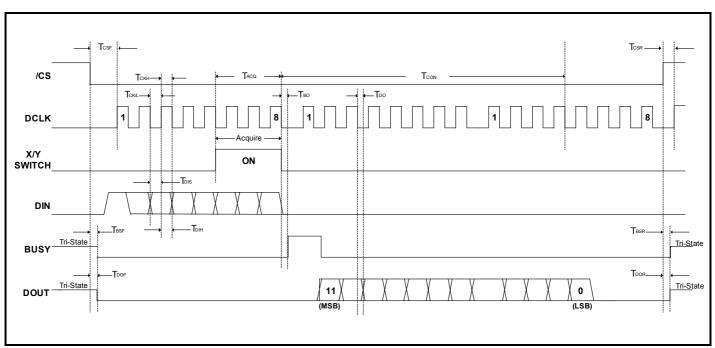


Figure 1. Timing Diagram of AR7643



FUNCTIONAL DESCRIPTION OVERVIEW

The AR7643 is a 12-bit switched-capacitor Analog-to-Digital (A/D) converter. The converter is fabricated on a 0.6µm CMOS process and packaged in the very small 16-pin SSOP package.

The typical operation of the AR7643 is shown in Figure 6. The AR7643 operates on a single supply ranging from +2.7V to +5.5V. It requires an external reference and an external clock. The reference voltage directly sets the input range of the converter.

The AR7643 contains four channel inputs, a serial interface, and low on-resistance switches for touch panel (see Block Diagram). The input to the converter is selected via the four-channel multiplexer as shown in Figure 5.

OPERATION OF 24-CLOCKS

The typical operation of AR7643's serial interface is shown in Figure 2. The AR7643 communicate with microprocessors or digital signal processors via a synchronous serial interface. One complete conversion can be accomplished with three serial communications, for a total 24 clock cycles on the DCLK input.

Serial Interface

The operation is initiated by a falling signal on Chip Select (/CS) input. After /CS falls the AR7643 look for a start bit on the DIN input. The first eight clock cycles are used to provide the control byte. At the end of the

operation the /CS pin should be brought high. Bringing /CS high after the conversion also minimizes supply current if DCLK is left running.

Control Byte

Table I and Table II are detailed information of the control byte (on DIN). The control byte provides the start operation, addressing, resolution, and power down information of the AR7643.

Start Bit - Initiate Start

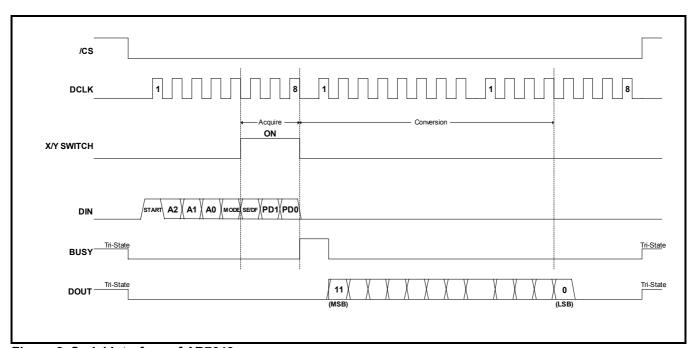
The control byte starts with the first high bit on DIN. The first bit must always be HIGH (1) to initiate the start of the conversion. The AR7643 will ignore any inputs on the DIN until the start bit is detected.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Start	A2	A1	A0	Mode1	Mode0	PD1	PD0

Table I. Control Bits in the Control Byte

BIT	NAME	DESCRIPTION
7	Start	Start Bit.
6, 5, 4	A2,A1,A0	Input Channel Select Bits.
3, 2	Mode1 Mode0	12-Bit / 8-Bit Conversion Configuration Bit.
1, 0	PD1,PD0	Power Down Control Bits

Table II. Description of the Control Bits



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Figure 2. Serial Interface of AR7643

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Addressing Bits - Input Channel Selection

The next three bits on control byte (A2, A1, A0) select the active input channel of the input multiplexer (see Table V, and Figure 5), and touch panel drivers.

Mode Bits - Conversion Resolution Configuration

The Mode bits (Mode1, Mode0) set the resolution of the analog-to-digital (ADC) converter. With the Mode1 bit LOW (0) the following conversion will have 12 bits of resolution. With the Mode1 bit HIGH (1) the following conversion will have 8 bits of resolution. See Table III for more information.

PD0 and PD1 Bits - Power Down Control

The last two bits (PD1, PD0) control the power-down mode of AR7643. If both bits are HIGH (1), the device is always powered up. If both bits are LOW (0), the device enters a power-down mode between conversions. See Table IV for more information.

OPERATION OF 16-CLOCKS

The typical operation of AR7643 is 24-clocks (three control bytes) per conversion. However the control bits for the next conversion can be overlapped with current conversion for a faster conversion. Figure 3 shows the timing of 16-Clocks per conversion.

Mode1	Mode0	DESCRIPTION
0	1	12bits Resolution
0	0	12bits Resolution
1	1	8bits Resolution
1	0	8bits Resolution

Table III. Resolution Configuration

PD1	PD0	PENIRQ	DESCRIPTION
0	0	Enable	Power-Down between conversions. Y- switch is on.
0	1	Disable	Power-Down between conversions. Y-switch is off. /PENIRQ is disabled
1	0	Disable	No used.
1	1	Disable	No Power-Down between conversions.

Table IV. Power-Down Selection

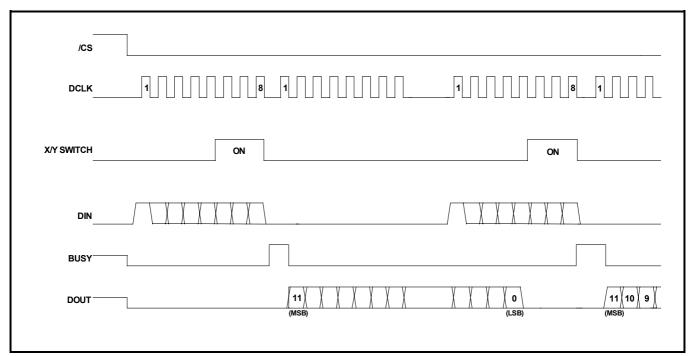


Figure 3. Timing of 16-clocks per Conversion

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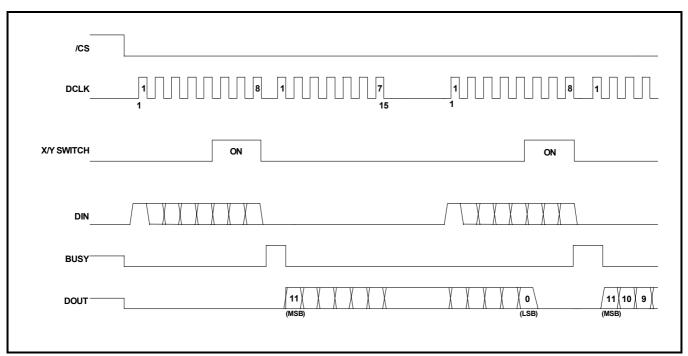


Figure 4. Timing of 15-clocks per Conversion

OPERATION OF 15-CLOCKS

The fastest operation (15-clocks per conversion) of AR7643 is shown on Figure 4. This operation will NOT work with the serial interface of most microcontrollers and digital signal processors, as they are not capable of providing 15 clocks cycles per serial transfer.

ANALOG INPUT

The AR7643 contains four channel inputs. X+ and Y+ inputs are for touch panel measurement, 2 auxiliary inputs are IN3 and IN4. The input to the A/D converter is selected via the four-channel multiplexer. (see Block Diagram section and Figure 5.)

Input Channel

Table V shown the input channel configuration of the AR7643. The control bits are set via the DIN pin. (see Control Byte section). The selected channel is for A/D converter input. Please refer to Figure 5 for detailed input channel multiplexer. For measuring X+ and Y+, Y switches and X switches are turned onrespectively.

Reference Input

The AR7643 requires an external reference voltage source. The reference input sets the Analog-to-Digital converter (ADC) input range. If the reference input is from the power supply directly, special care must be taken to avoid noise from power supply.

A2	A 1	A 0	Input Channel.	X Switch	Y Switch	Reference
0	0	1	X+	OFF	ON	V_{REF}
1	0	1	Y+	ON	OFF	V_{REF}
0	1	0	IN3	OFF	OFF	V_{REF}
1	1	0	IN4	OFF	OFF	V_{REF}

Table V. Input Channel Configuration

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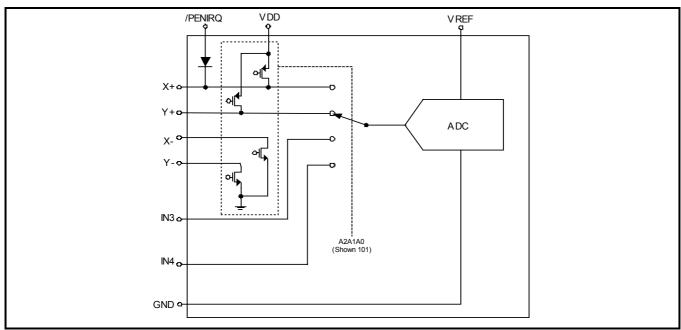


Figure 5. Diagram of Input Channel

Typical Operating Circuit

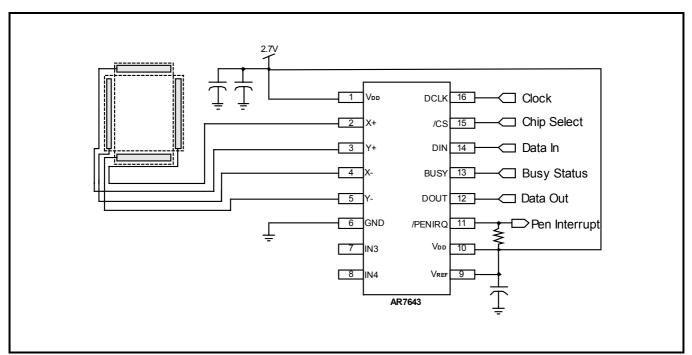


Figure 6. Typical Operation of The AR7643

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APPLICATION CONSIDERATIONS

Resistive Touch Panel (4-Wire)

The 4-wire resistive touch panel consists of 2 resistive plates that are separated by a small gap. Each of the panel has a resistance in the range from 200 to 2000 ohms.

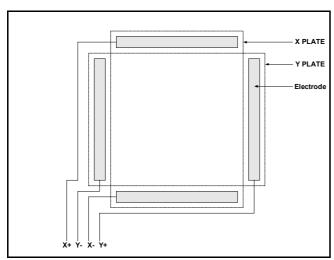


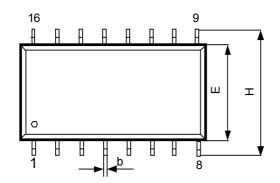
Figure 7. 4-wire Resistive Touch Panel

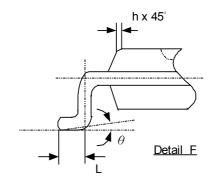
The panel works by applying a voltage across the X plate or Y plate resistive networks. If a voltage is applied, for example, between X+ and X- then a voltage divider is formed on the X plate. When the Y plate is touched to the X plate, a voltage will be developed on the Y plate. By accurately measuring this voltage, the position of the panel can be determined. The connection of AR7643 to the touch panel should be as short as possible.

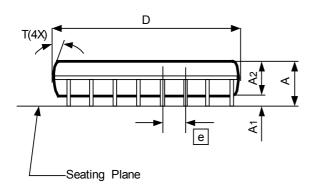


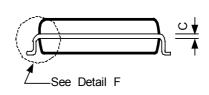
Package Information

The Package of AR7643 is 16-pin SSOP.









SYMBOLS	DIN	MENSIONS (MM)	DIMENSIONS (MIL)		
OTHIDOLO	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.35	1.60	1.75	53	63	68
A 1	0.10	0.15	0.25	4	6	10
A 2			1.50			59
b	0.20	0.254	0.30	8	10	12
С	0.18	0.203	0.25	7	8	10
D	4.80	4.90	5.00	189	193	197
E	3.80	3.90	4.00	150	154	157
Н	5.80	6.00	6.80	228	236	244
e	0.6358 BSC				25 BSC	
L	0.40	0.635	1.27	16	25	50
h	0.25	0.42	0.50	10	17	20
θ	0°		8°	0 °		8°





Notes:

This is preliminary datasheet on a new product now in development.

Details are subject to change without notice.