LVDS Product

DTC34LM85AL *(Rev. 1.0)*

REVISED APR. 2009

+3.3V LVDS 24Bit Flat Panel Display (FPD) Transmitter - 85MHz

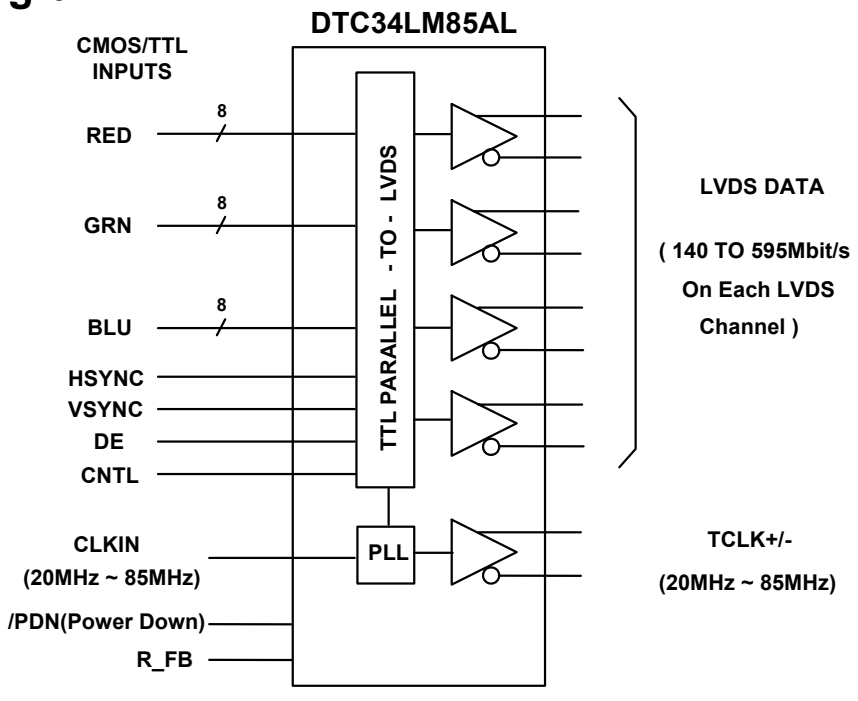
General Description

The DTC34LM85AL transmitter converts 28 bits of CMOS/TTL data into four LVDS(Low Voltage Differential Signaling) data streams. A CLKIN signal is phase-locked and transmitted in parallel with the data streams over a fifth LVDS link. 24 bits of graphic data and 3 bits of timing and 1 control data are transmitted at a rate of 595 Mbps per LVDS data channel at a transmit clock frequency of 85MHz. Using a 85 MHz clock, the data throughput is 297.5 Mbytes/sec. The R_FB pin selects either rising or falling edge trigger of CLKIN. A Rising/Falling edge strobe transmitter will interoperate with a Rising/Falling edge strobe receiver (DTC34LF/R86L) without any translation logic. This chipset is an ideal means to solve EMI and cable size problems associated with wide, high speed TTL interfaces.

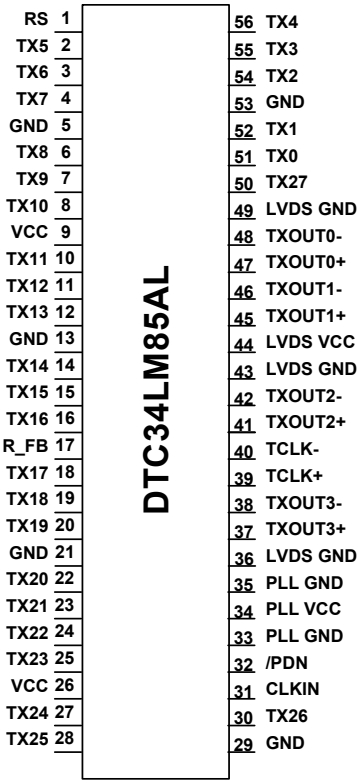
Features

- Wide frequency range : 20 to 85 MHz shift clock support
- Narrow bus (10 lines) reduces cable size and cost
- Single 3.3V supply
- Power-Down Mode
- Supports VGA, SVGA, XGA and SXGA
- Supports Spread Spectrum Clock Generator
- On Chip Input Jitter Filtering
- Up to 297.5 Megabytes/sec bandwidth
- Reduced Swing LVDS Support for low EMI
  (200mV or 350mV Swing LVDS Selectable)
- PLL requires no external components
- Low profile 56 lead TSSOP package (PB Free)
- Compatible with TIA/EIA-644 LVDS standard
- Compatible with National DS90C385
  Thine THC63LVDM83R

Block Diagram



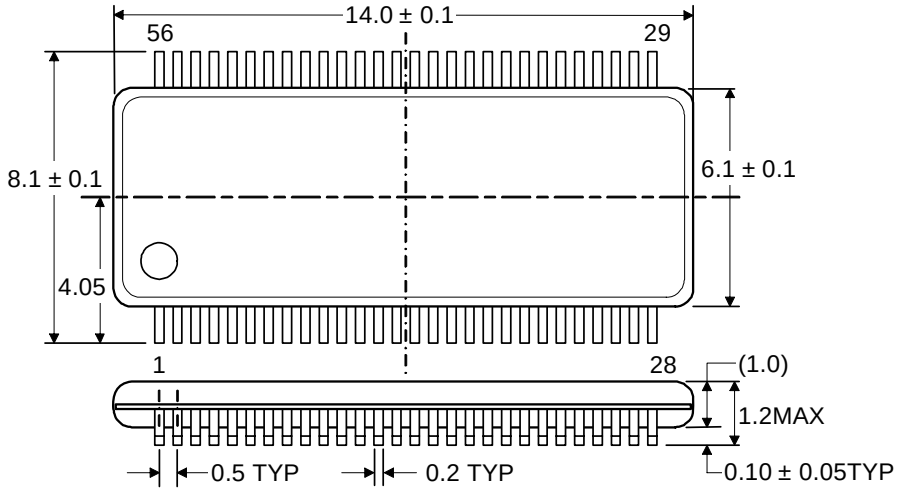
PIN OUT



PACKAGE

56 Lead Molded Thin Shrink Small Outline Package, JEDEC

Unit : millimeters



Electrical Characteristics

Vcc=3.0 ~ 3.6V, Ta=-10 ~ +70°C

CMOS/TTL DC SPECIFICATIONS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage		2.0		Vcc	V
V_{IL}	Low Level Input Voltage		GND		0.8	V
I_{IN}	Input Current	$0V \le V_{IN} \le Vcc$			±10	uA
I_{PD}	Pull Down Current	R_FB pin, VIH=Vcc			10	uA

LVDS TRANSMITTER DC SPECIFICATIONS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OD}	Differential Output Voltage, Normal RS=VCC (Small RS=GND)	RL=100Ω	250 (100)	350 (200)	450 (300)	mV
ΔV_{OD}	Change in V_{OD} between Complimentary Output States				35	mV
V_{OC}	Common Mode Voltage		1.125	1.25	1.375	V
ΔV_{OC}	Change in V_{OC} between Complimentary Output States				35	mV
I_{OZ}	Output TRI-STATE Current	/PDN=0V, Vout=0 to Vcc			±10	uA

TRANSMITTER SUPPLY CURRENT

Symbol	Parameter	Conditions	Typ	Max	Units
ICC_{TG}	Transmitter Supply Current (16 Grayscale)	RL=100Ω, CL = 10pF, f = 85MHz RS=VCC (RS=GND)	36 (31)		mA
ICC_{TW}	Transmitter Supply Current (Worst Case)	RL=100Ω, CL = 10pF, f = 85MHz RS=VCC (RS=GND)	39 (34)		mA
ICC_{TP}	Transmitter Supply Current (Power Down)	/PDN=0V	10		uA

* All typical values are Vcc = 3.3V, Ta = 25°C

Absolute Maximum Ratings (Note1)

Supply Voltage (Vcc)	-0.3 to +4.0V
CMOS/TTL Input Voltage	-0.3V to (Vcc + 0.3V)
CMOS/TTL Output Voltage	-0.3V to (Vcc + 0.3V)
LVDS Driver Output Voltage	-0.3V to (Vcc + 0.3V)
Output Short Circuit Duration	Continuous
Junction Temperature	+150 °C
Storage Temperature Range	-65 °C to 150 °C
Lead Temperature (Soldering, 4 sec.)	+260 °C
Maximum Power Dissipation @25°C	1.4W

(Note 1)

"Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation

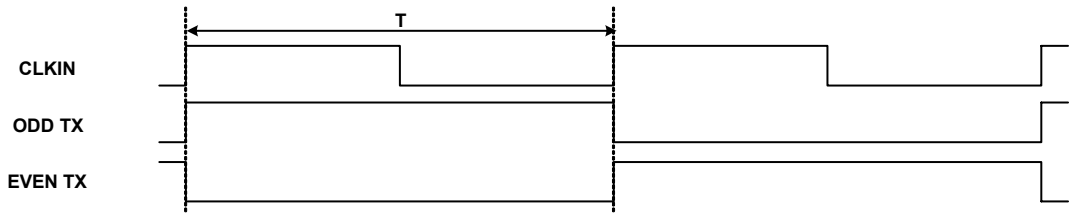
Transmitter Switching Characteristics

Vcc=3.0 ~ 3.6V, Ta=-10 ~ +70°C, T=1/f

Symbol	Parameter	Min	Typ	Max	Units
t_{TCIT}	CLKIN Transition Time			5.0	nS
t_{TCP}	CLKIN Period	11.76	T	50	nS
t_{TCH}	CLKIN High Time	0.35T	0.5T	0.65T	nS
t_{TCL}	CLKIN Low Time	0.35T	0.5T	0.65T	nS
t_{TCD}	CLKIN to TCLK+/- Delay		2T/7 + 2.3		nS
t_{TS}	TTL Data Setup to CLKIN	2.5			nS
t_{TH}	TTL Data Hold from CLKIN	2.5			nS
t_{LVT}	LVDS Transition Time		0.6	1.5	nS
t_{TDP1}	Transmitter Output Data Position 0 (85MHz)	-0.2	0	0. 2	nS
t_{TDP0}	Transmitter Output Data Position 1 (85MHz)	T/7-0. 2	T/7	T/7+0. 2	nS
t_{TDP6}	Transmitter Output Data Position 2 (85MHz)	2T/7-0. 2	2T/7	2T/7+0. 2	nS
t_{TDP5}	Transmitter Output Data Position 3 (85MHz)	3T/7-0. 2	3T/7	3T/7+0. 2	nS
t_{TDP4}	Transmitter Output Data Position 4 (85MHz)	4T/7-0. 2	4T/7	4T/7+0. 2	nS
t_{TDP3}	Transmitter Output Data Position 5 (85MHz)	5T/7-0. 2	5T/7	5T/7+0. 2	nS
t_{TDP2}	Transmitter Output Data Position 6 (85MHz)	6T/7-0. 2	6T/7	6T/7+0. 2	nS
t_{TPLLS}	Transmitter Phase Lock Loop Set	-	-	10	mS

AC Timing Diagrams

FIGURE 1. Test Pattern "Worst Case Pattern"



AC Timing Diagrams(Continued)

FIGURE 2. Test Pattern "16 Grayscale Test Pattern"

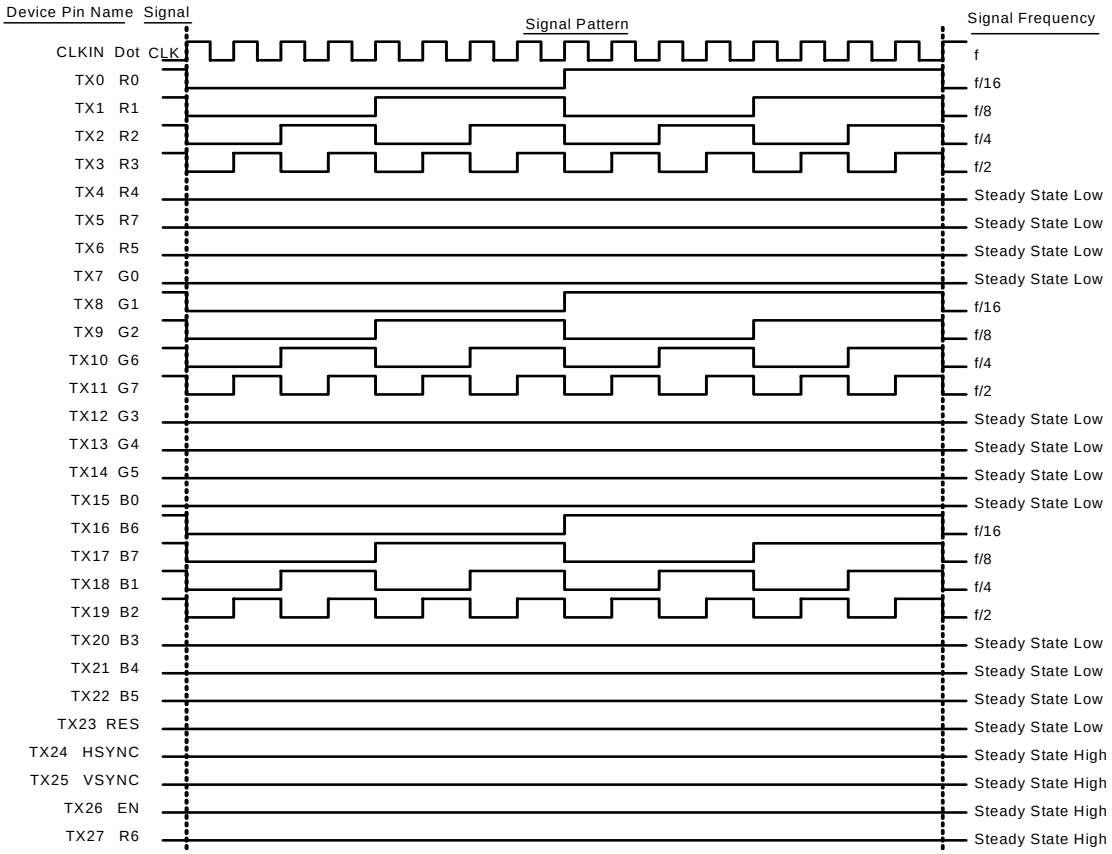


FIGURE 3. TTL Input

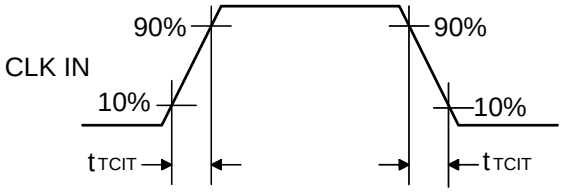
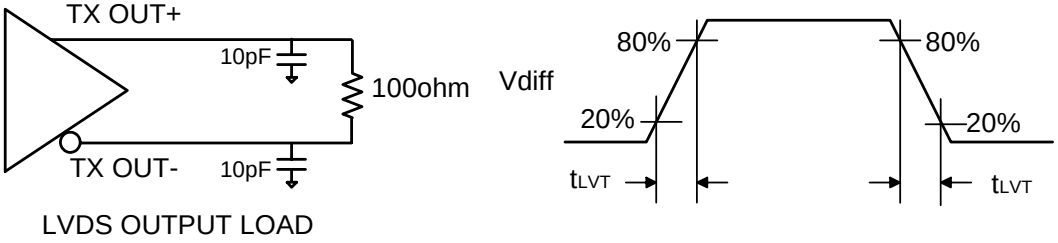


FIGURE 4. LVDS Output

Vdiff= (TXOUT+) – (TXOUT–)



AC Timing Diagrams (Continued)

FIGURE 5. Phase Lock Loop Set Time

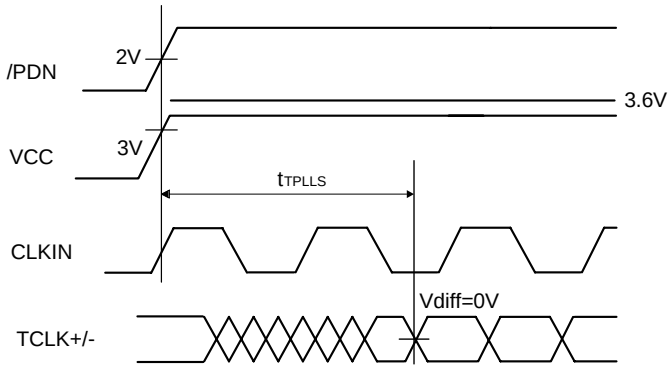
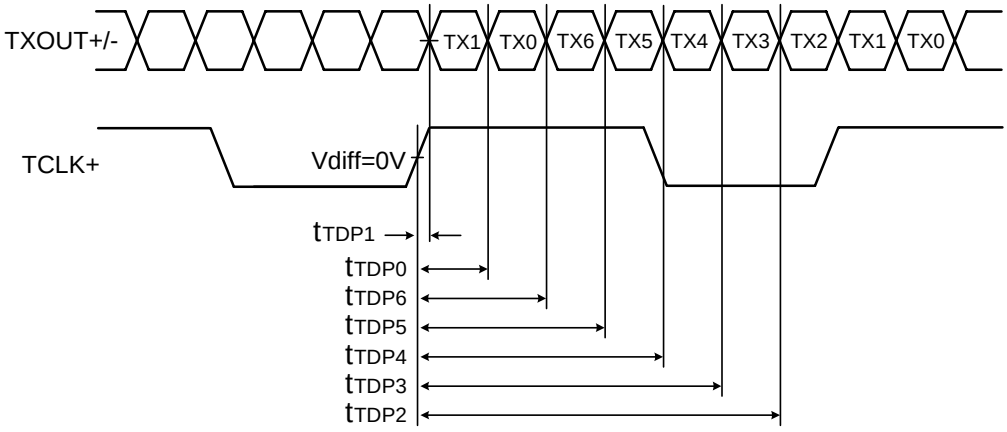


FIGURE 6. Transmitter Device Operation



Note : **1) Vdiff = (TXOUT+) - (TXOUT-), ... (TCLK+) – (TCLK-)**

FIGURE 7. Parallel TTL Data Inputs Mapped to LVDS Outputs – DTC34LM85AL

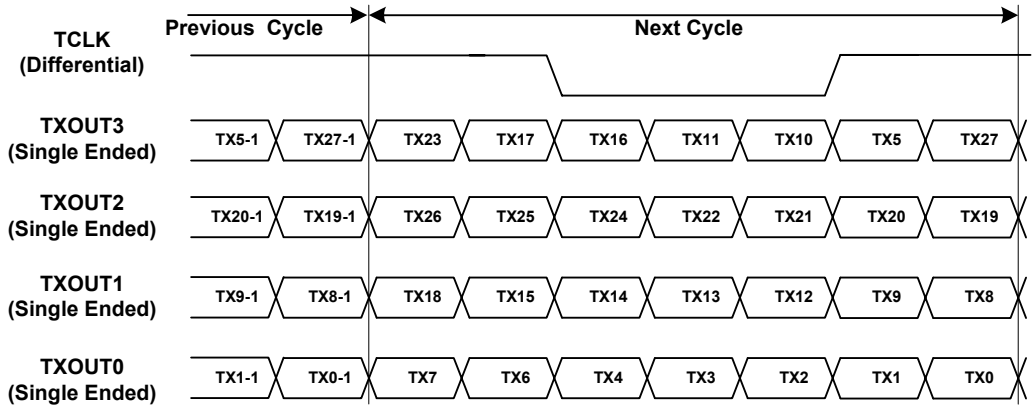
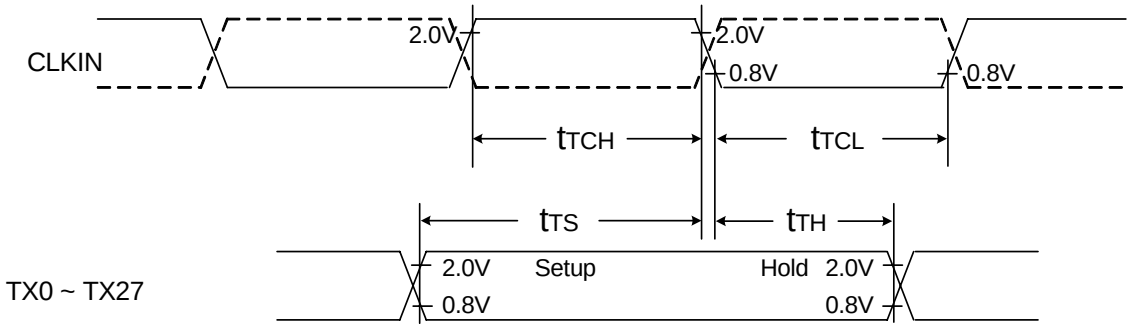


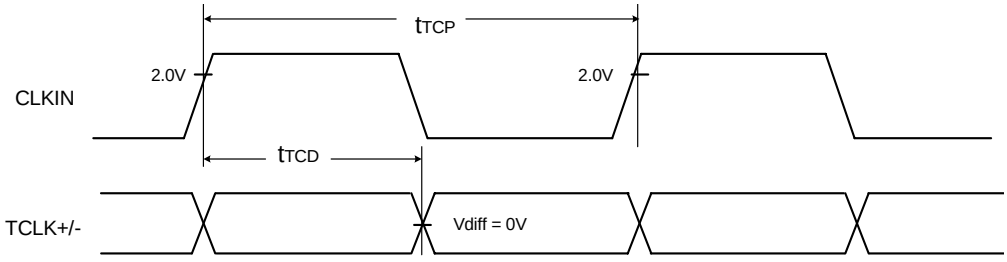
FIGURE 8. Setup/Hold and High/Low Times



Note : **1) CLKIN : for DTC34LM85AL(R_FB=GND), denoted as solid line**

for DTC34LM85AL(R_FB=VCC), denoted as dotted line

FIGURE 9. CLKIN to CLKOUT Delay



Note : **1) Vdiff = (TXOUT+) - (TXOUT-), ... (TCLK+) - (TCLK-)**

FIGURE 10. Package Pin Description

Pin Name	Pin #	Type	Description
TXOUT0-, TXOUT0+	48, 47	LVDS OUT	LVDS differential data outputs.
TXOUT1-, TXOUT1+	46, 45	LVDS OUT	
TXOUT2-, TXOUT2+	42, 41	LVDS OUT	
TXOUT3-, TXOUT3+	38, 37	LVDS OUT	
TCLK-, TCLK+	40, 39	LVDS OUT	LVDS differential clock outputs.
TX0 ~ TX6	51,52,54,55,56,2, 3	IN	TTL level data inputs. This includes : 8 Red, 8 Green, 8 Blue, and 4 control lines (HSYNC, VSYNC, DE, CNTL)
TX7 ~ TX13	4,6,7,8,10,11,12	IN	
TX14 ~ TX20	14,15,16,18,19,20,22	IN	
TX21 ~ TX27	23,24,25,27,28,30,50	IN	
CLK IN	31	IN	TTL level clock input. This falling edge acts as data strobe
/PDN	32	IN	TTL level input. H : Normal operation L : Power down (all output are low)
R_FB	17	IN	Programmable strobe select. H:Rising edge, L :Falling edge
RS	1	IN	LVDS Swing Control (Normal RS=VCC, Small RS=GND)
VCC	9,26	Power	Power supply pins for TTL inputs.
GND	5,13,21,29,53	Ground	Ground pins for TTL inputs.
LVDS VCC	44	Power	Power supply pin for LVDS outputs.
LVDS GND	36,43,49	Ground	Ground pins for LVDS outputs.
PLL VCC	34	Power	Power supply pin for PLL.
PLL GND	33,35	Ground	Ground pin for PLL.

IMPORTANT NOTICE :

- The contents of this data sheet are subject to change without prior notice.

DOESTEK Co., Ltd. (www.doestek.co.kr)

6F TechnoComplex Korea Univ., Anam-Dong5-Ga, Songbuk-Gu, SEOUL, KOREA Tel) 82-2-926-9464