64Gb Based NAND Flash

64Gb and 128Gb NAND Flash Specification

Document Title

Revision History

Revision No.	History	Draft Date	Remark
1.0	- Release	Aug. 2013	

Base product: 64Gb NAND Flash

■ **Multilevel Cell technology**

■ **NAND INTERFACE**
  - x8 bus width

■ **Supply Voltage**
  - Vcc : 2.7V ~ 3.6V

■ Organization
  - (16,384+1,664)bytes x 256pages x 1,060blocks x 2plane
  - Page size : 16,384+1,664bytes
  - Block size : 256pages x (4M+416K) bytes
  - Plane size : (1,024blocks + 36 block)/1plane

■ **Page Read / Program Time**
  - Random Read Time(tR) : 90 us
  - Sequential Access (tRC/tWC) : 16ns(Min.)
   (Read/Write throughput per pin : up to 50MHz)
  - Page Program Time : 1.5 ms

■ **Block Erase**
  - Block Erase Time : 5 ms (Typ)

■ **ECC Requirement**
40bit correction /1KByte

■ **Operating Current**
  - Page Read : 50 mA (max)
  - Page Program : 50 mA (max)
  - Block Erase: 50 mA (max)
  - Standby (CMOS): 50uA (max)

■ **Hardware Data Protection**
  - Program/Erase locked during power transitions

■ **Package**
  - T-SOP   :Size : 12x20mm
  - Pin count   : 48
  - 64Gbit: single die stack, H27UCG8T2ETR-BC
  - 128Gbit: two-die stack, H27UDG8U2ETR-BC (TBD)

CONTENTS

1. Summary Description

The product part No. H27UCG8T2ETR-BC is a 3.3V 64Gbit NAND flash memory and H27UDG8U2ETR-BC is a double die 128Gbit NAND flash memory. The Device contains 2 planes in a single die. Each plane is made up of the 1,060 blocks. Each block consists of 256 programmable pages. Each page contains 16,384 data bytes + 1,664 spare bytes. The pages are subdivided into an 16,384 byte main data storage area with a spare 1,664 byte district.
Page program operation can be performed in typical 1500us, and a single block can be erased in typical 5ms.

1. 1. Product List

Table1-1. List of supported versions / packages

Product information				
P/N	Density	Vcc	Operating range	PACKAGE
H27UCG8T2ETR-BC	64Gb	3.3V	2.7 to 3.6V	48pin TSOP
H27UDG8U2ETR-BC (TBD)	128Gb			

1.2. PIN DESCRIPTION

Table 1-2. Signal description

Pin Name	Type	Description
I/O 0 - I/O 7	Input	**DATA INPUTS/OUTPUTS** The I/O pins is used to COMMAND LATCH cycle, ADDRESS INPUT cycle, and DATA in-out cycles during read / write operations. The I/O pins float to High-Z when the device is deselected or the outputs are disabled.
CLE	Input	**COMMAND LATCH ENABLE** This input activates the latching of the I/O inputs inside the Command Register on the Rising edge of Write Enable ($\overline{WE}$).
ALE	Input	**ADDRESS LATCH ENABLE** This input activates the latching of the I/O inputs inside the Address Register on the Rising edge of Write Enable ($\overline{WE}$).
$\overline{CE}$	Input	**CHIP ENABLE** This input controls the selection of the device. When the device is busy, $\overline{CE}$ low does not deselect the memory. The device goes into Stand-by mode when $\overline{CE}$ goes High during the device is in Ready state. The $\overline{CE}$ signal is ignored when device is in Busy state, and will not enter Standby mode even if the $\overline{CE}$ goes high.
$\overline{WE}$	Input	**WRITE ENABLE** This input acts as clock to latch Command, Address and Data. The I/O inputs are latched on the rise edge of $\overline{WE}$.
$\overline{RE}$	Input	**READ ENABLE** The $\overline{RE}$ input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of $\overline{RE}$ which also increments the internal column address counter by one.
$\overline{WP}$	Input	**WRITE PROTECT** The $\overline{WP}$ pin, when Low, provides a hardware protection against undesired write operations. Hardware Write Protection is activated when the Write Protect pin is low. In this condition modify operation do not start and the content of the memory is not altered. Write Protect pin is not latched by Write Enable to ensure the protection even during the power up phases.
R/$\overline{B}$	Output	**READY / BUSY** The Ready/Busy output is an Open Drain pin that signals the state of the memory.

VCC	Supply	**POWER SUPPLY VOLTAGE PIN** The VCC supplies the power for all the operations. (Read, Write, and Erase).
VSS	Supply	**GROUND CONNECTION PIN**
NC		**NO CONNECTED**

NOTE:

A 0.1uF capacitor be connected between the Vcc (Supply Voltage) pin and the Vss (Ground) pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during program and erase operations.

1.3. Pin Diagram

Figure 1-1. Pin diagram
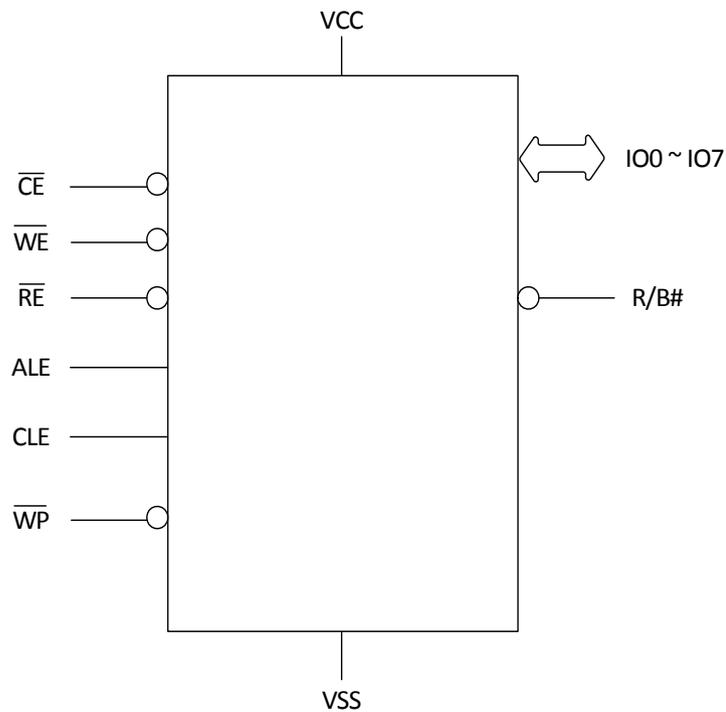
1.4. Pin Assignments

Figure 1-2. 48-pin TSOP
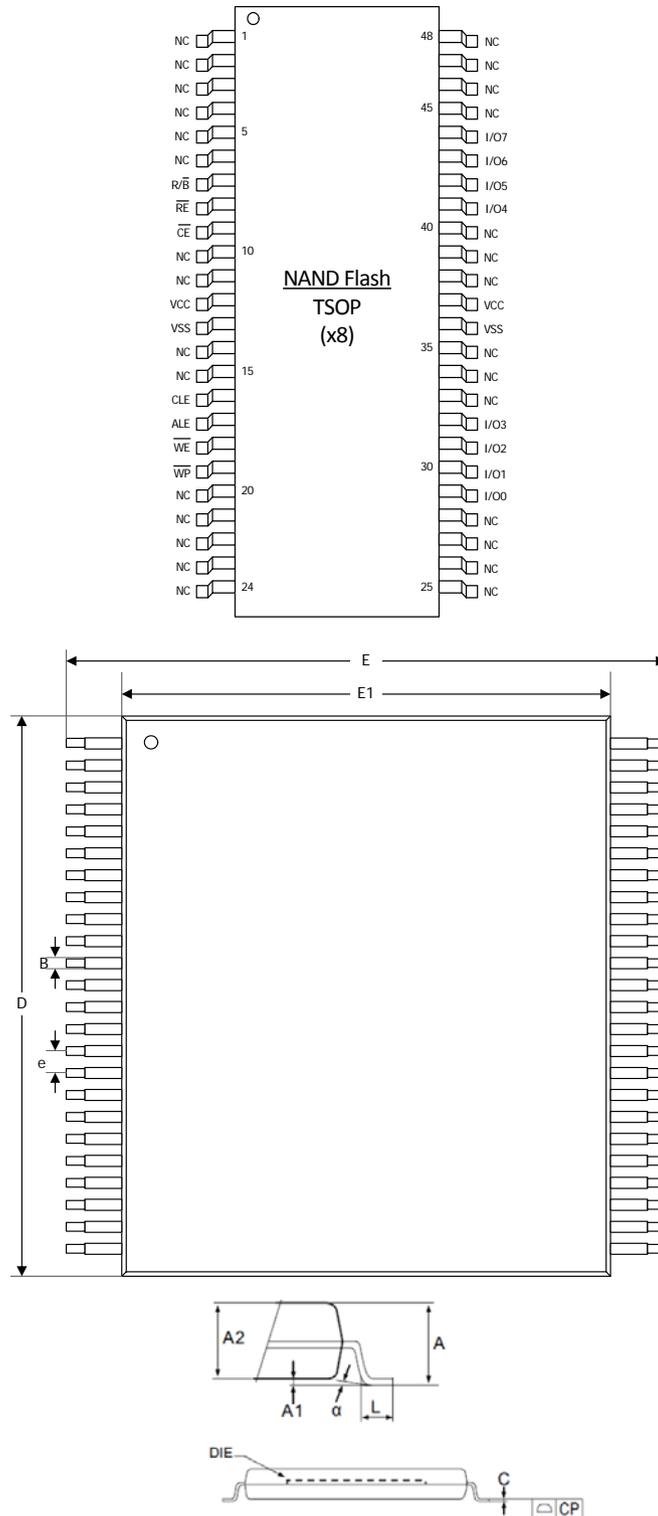
Table 1-3. 48-pin TSOP, Package Mechanical Data

Symbol	Milimeters			Symbol	Milimeters		
	Min	**Typ**	**Max**		**Min**	**Typ**	**Max**
A	-	-	1.200	D	11.91	12.00	12.12
A1	0.050	-	0.150	E	19.90	20.00	20.10
A2	0.980	-	1.030	E1	18.30	18.40	18.50
B	0.170	-	0.250	e	-	0.500	-
C	0.100	-	0.200	L	0.50	-	0.68
Symbol	**Milimeters**			**Symbol**	**Milimeters**		
	Min	**Typ**	**Max**		**Min**	**Typ**	**Max**
alpha	0	-	5	CP	-	-	0.10

1.5. Block Diagram

Figure 1-3. Block diagram
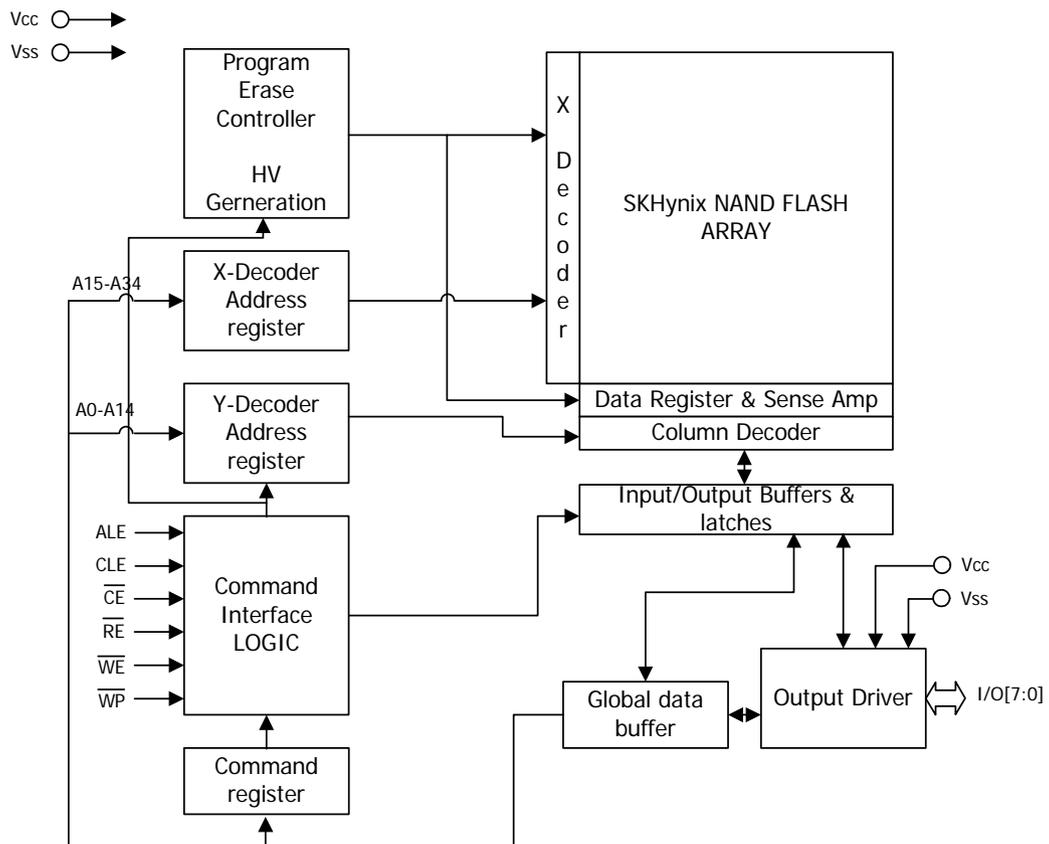
1.6. Array Organization

Figure 1-4. Array organization

NOTE :
1) H27UCG8T2ETR (8GByte) single die stack

1.7. Addressing

Table 1-4. Array organization

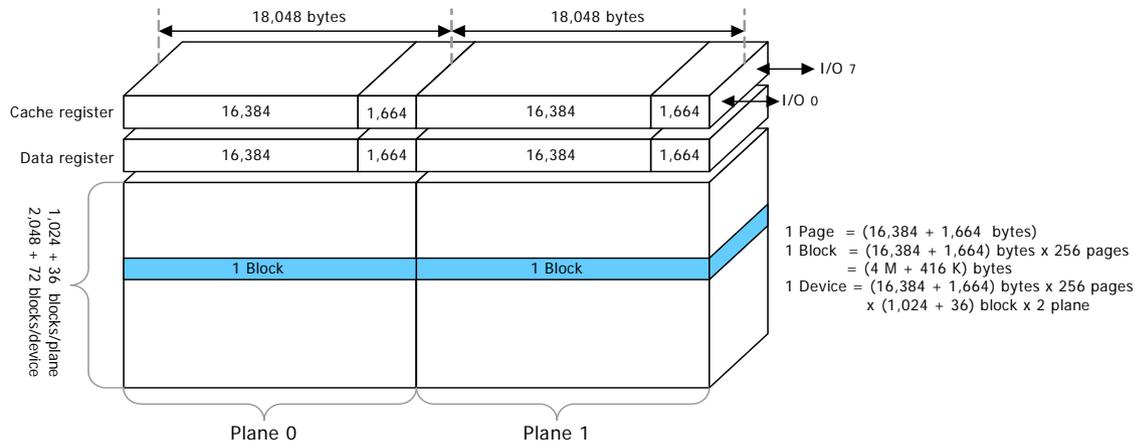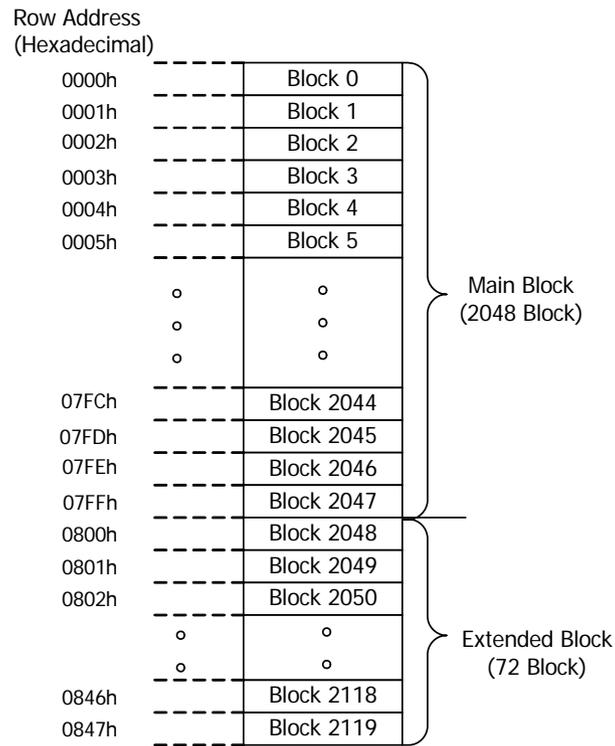| Bus Cycle	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7	Address information		
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7	Column		A[14:0]
2nd Cycle	A8	A9	A10	A11	A12	A13	A14	L[1]			
3rd Cycle	A15	A16	A17	A18	A19	A20	A21	A22	Row	Page	A[22:15]
4th Cycle	A23	A24	A25	A26	A27	A28	A29	A30		Plane	A[23]
5th Cycle	A31	A32	A33	A34	A35[2]	A36[2]	L[1]	L[1]		Block	A[34:24]

Notes:
1. L must be set to Low.
2. A35 and A36 are invalid.
3. Only Block0 to Block 2119 are valid physical block addresses. The device ignores any additional address input cycle than required.

1.7.1. Extended Block Arrangement

The device offer 72 extended blocks to increase valid blocks.

Row Address
(Hexadecimal)

Row Address	Block
0000h	Block 0
0001h	Block 1
0002h	Block 2
0003h	Block 3
0004h	Block 4
0005h	Block 5
○	○
07FCh	Block 2044
07FDh	Block 2045
07FEh	Block 2046
07FFh	Block 2047
0800h	Block 2048
0801h	Block 2049
0802h	Block 2050
○	○
0846h	Block 2118
0847h	Block 2119

Main Block (2048 Block)

Extended Block (72 Block)

1.7.2. Valid Block

Table 1-5. The number of valid block

Part No.	Density	Symbol	Min	Typ.	Max	Unit
H27UCG8T2ETR-BC	16Gbit	NVB	1997	2048	2120	Blocks

Notes:
1. The 1st block is guaranteed to be a valid block at the time of shipment.
2. This single device has a maximum of 2120 invalid blocks.
3. Invalid blocks are one that contains one or more bad bits. The device may contain bad blocks on shipment.

1.8. Command Set

Table 1-6. Command Set table

	1st CYCLE	Number of Address cycles	Data Input cycles	2nd CYCLE	Number of Address cycles	Data Input cycles	3rd CYCLE	Acceptable command during busy
PAGE READ	00h	5	-	30h	-	-	-	No
READ FOR COPY-BACK	00h	5	-	35h	-	-	-	No

	1st CYCLE	Number of Address cycles	Data Input cycles	2nd CYCLE	Number of Address cycles	Data Input cycles	3rd CYCLE	Acceptable command during busy
RANDOM DATA OUTPUT [1]	05h	2	-	E0h	-	-	-	No
SINGLE/MULTI-PLANE CACHE READ [5]	31h	-	-	-	-	-	-	No
SINGLE/MULTI-PLANE CACHE READ END [5]	3Fh	-	-	-	-	-	-	No
READ ID	90h	1	-	-	-	-	-	No
READ STATUS REGISTER	70h	-	-	-	-	-	-	Yes
PAGE PGM (start)/ CACHE PGM [5] (end)	80h	5	Yes	10h	-	-	-	No
RANDOM DATA INPUT[1]	85h	2	Yes	-	-	-	-	No
COPY-BACK PGM	85h	5	Option	10h	-	-	-	No
CACHE PGM (start)[5]	80h	5	Yes	15h	-	-	-	No
BLOCK ERASE	60h	3	-	D0h	-	-	-	No
RESET	FFh	-	-	-	-	-	-	Yes
MULTI-PLANE PAGE READ	60h	3	-	60h	3	-	30h	No
MULTI-PLANE CACHE READ START [5] [6]	60h	3	-	60h	3	-	33h	No
MULTI-PLANE READ FOR COPY-BACK	60h	3	-	60h	3	-	35h	No
MULTI-PLANE BLOCK ERASE	60h	3	-	60h	3	-	D0h	No
MULTI-PLANE RANDOM DATA OUTPUT [1] [3]	00h	5	-	05h	2	-	E0h	No
MULTI-PLANE READ STATUS REGISTER	78h	3	-	-	-	-	-	Yes
MULTI-PLANE READ STATUS REGISTER (legacy)	75h	-	-	-	-	-	-	Yes
MULTI-PLANE PAGE PGM/ MULTI-PLANE CACHE PGM (end)	80h	5	Yes	11h-81h [2]	5	Yes	10h	No
MULTI-PLANE COPY-BACK PGM	85h	5	Option	11h-81h [2]	5	Option	10h	No
MULTI-PLANE CACHE PGM (start) [5]	80h	5	Yes	11h-81h [2]	5	Yes	15h	No
CACHE READ ENHANCED	00h	5	-	31h	-	-	-	No
MULTI-PLANE CACHE READ ENHANCED	60h	3	-	60h	3	-	31h	No

Notes:
1. Random Data Input/Output must be performed in a selected page.
2. Any command between 11h and 81h is prohibited except 70h, 78h, 75h and FFh.
3. Multi-plane Random data-out must be used after multi-plane read operations
(Multi-plane Page Read, Multi-plane Cache Read and Multi-plane Read for Copy Back).
4. Do not change plane address order when using all multi-plane operations.

5. All cache operation (cache program, cache read) is available only within a block.
6. It's possible to confirm the multi-plane cache read first step using both 30h and 33h.

Caution:
1. Any undefined command inputs are prohibited except for above command set.
2. Multi-plane page read, multi-plane cache read, and multi-plane read for copy-back must be used
after multi-plane programmed page, multi-plane cache program, and multi-plane copy-back program.

1.9. Mode Selection

Table 1-7. Command Set table

CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$	Mode	
H	L	L	Rising	H	X	Read Mode	Command Input
L	H	L	Rising	H	X		Address Input (5 Cycles)
H	L	L	Rising	H	H	Write Mode	Command Input
L	H[1]	L	Rising	H	H		Address Input (5 Cycles)
L	L	L	Rising	H	H	Data Input	
L	L[1]	L	H	Falling	X	Sequential Read and Data Output	
L	L	L	H[3]	H[3]	X	During Read (Busy)	
X	X[1]	X	X	X	H	During Program (Busy)	
X	X	X	X	X	H	During Erase (Busy)	
X	X	X	X	X	L	Write Protect	
X	X	H	X	X	0V/Vcc[2]	Stand-By	

Notes:
1. X can be VIL or VIH. H = Logic level "High". L = Logic level "Low".
2. WP should be biased to CMOS high or CMOS low for stand-by mode.
3. WE and RE during Read Busy must be keep on high to prevent unplanned command/address/data input or to avert unin-
tended data out. In this time, only Reset, Read Status, and Multi-plane Read Status can be inputted to the device.

2. Electrical Characteristics

2.1. Absolute Maximum Ratings

Table 2-1. Absolute maximum ratings

Item	Symbol	Value Min	Unit
Ambient Operating Temperature (Commercial Temperature Range) *P/N: H27UCG8T2ETR-BC	TA	0 to +70	degree
Ambient Operating Temperature (Industrial Temperature Range) *P/N: H27UCG8T2ETR-BI		-40 to +85	
Temperature Under Bias	TBIAS	-50 to +125	
Storage Temperature	TSTG	-65 to +150	
Input or Output Voltage	VIO	-0.6 to 4.6	V
Supply Voltage	VCC	-0.6 to 4.6	

Notes:
1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.
2. Minimum voltage may undershoot to -2V during transition and for less than 20ns during transitions.
   Maximum voltage may overshoot to Vcc+2V during transition and for less than 20ns during transitions.

2.2. Recommended DC Operating Conditions

Table 2-2. Recommended DC operating conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	VCC	2.7	3.3	3.6	V
Ground voltage supply	VSS	0	0	0	V

2.3. Capacitance

The input capacitance requirements are defined in nest Table. The TSOP testing conditions that be used to verify the input capacitance requirements are: temperature of 25 degrees, VIN = 0V, and a frequency of 1MHz.

Table 2-3. TSOP Input/ Output capacitance (TA=25C, VCC=3.3V, f=100MHz)

Item	Symbol	Test Condition	Device	Min	Max	Unit
Input/Output Capacitance	CI/O	VIL=0V	H27UCG8T2ETR H27UDG8U2TR	-	10	pF
Input Capacitance	CIN	VIN=0V		-	10	

2.4. Electrical DC and Operating Characteristics

Table 2-4. DC Characteristics

Parameter		Symbol	Test Conditions	H27UCG8T2ETR-BC			Units
				Typ	Typ	Max	
Power on reset current		ICC0	FFh command input after power on	-	-	50	mA
Operating Current	Read	ICC1	tRC= tRC(min), CE#=VIL, IOUT=0 mA	-	-	50	mA
	Program	ICC2	-	-	-	50	mA
	Erase	ICC3	-	-	-	50	mA
Stand-by Current (CMOS)		ICC5	CE#=VCC-0.2, WP#=0V/VCC	-	10	50	mA
Input Leakage Current		ILI	VIN=0 to VCC(MAX)	-	-	+/-10	uA
Output Leakage Current		ILO	VOUT=0 to VCC(MAX)	-	-	+/-10	uA
Input High Voltage		VIH	-	VCC*0.8	-	VCC+0.3	V
Input Low Voltage		VIL	-	-0.3	-	0.2*VCC	V
Output High Voltage Level		VOH	IOH=-400uA	2.4	-	-	V
Output Low Voltage Level		VOL	IOL=2.1mA	-	-	0.4	V
Output Low Current (R/B#)		IOL (R/B#)	VOL=0.4V	8	10	-	mA

2.5. Program/ Read / Erase Characteristics

Table 2-5. Program/ Read / Erase Characteristics

Parameter	Symbol	Typ.	Max	Unit
Program (following 10h)	tPROG	1500	4000	uS
Cache Program (following 15h)	tCBSYW	-	4000	uS
Multi-plane Program / Multi-plane Cache Program / Multi-plane Copy-back Program (following 11h)	tDBSY	0.5	3	uS
Cache Read / Multi-plane Cache Read (following 31h/3Fh)	tCBSYR	-	90	uS
Block Erase / Multi-plane Block Erase	tBERS	5	10	mS
Number of partial Program Cycles in the same page	NOP	-	1	Cycle

Notes:
Typical value is measured at VCC=3.3V, TA=25C. Not 100% tested.

2.6. AC Test condition

Table 2-6. AC Test Conditions

Parameter	Value
Input Pulse Levels	0 V to VCC
Input Rise and Fall Times	5nm
Input and Output Timing Levels	VCC*0.5
Output Load (2.7V-3.6V)	CL= 50pF

Note:
These parameters are verified device characterization and are not 100% tested.

2.7. AC Characteristics for Command, Data and Address Input

Table 2-7. Parameter Descriptions

Parameter	Symbol	H27UCG8T2ETR-BC H27UDG8U2ETR-BC		Unit
		Min	Max	
CLE setup time	tCLS	6	-	ns
CLE Hold time	tCLH	3	-	ns
CE setup time	tCS	20	-	ns
CE hold time	tCH	5	-	ns
WE pulse width	tWP	8	-	ns
ALE setup time	tALS	6	-	ns
ALE hold time	tALH	3	-	ns
Data setup time	tDS	6	-	ns
Data hold time	tDH	2	-	ns
Write cycle time	tWC	16	-	ns
WE high hold time	tWH	6	-	ns
Data transfer from cell to register	tR	-	90	ns
ALE to RE delay	tAR	10	-	ns
CLE to RE delay	tCLR	10	-	ns
Ready to RE low	tRR	20	-	ns
RE pulse width	tRP	8	-	ns
WE high to busy	tWB	-	100	ns
Read cycle time	tRC	16	-	ns
RE access time	tREA	-	16	ns
RE high to output high Z	tRHZ	-	100	ns
CE high to output high Z	tCHZ	-	50	ns

Parameter	Symbol	H27UCG8T2ETR-BC H27UDG8U2ETR-BC		Unit
		Min	Max	
RE high to output hold	tRHOH	15	-	ns
RE low to output hold	tRLOH	5	-	ns
RE or CE high to output hold	tCOH	15	-	ns
RE high hold time	tREH	6	-	ns
WE high to RE low	tWHR	80	-	ns
WE high to RE low for Random data out	tWHR2	200	-	ns
RE high to WE low	tRHW	100	-	ns
Output high Z to RE low	tIR	0	-	ns
CE low to RE low	tCR	10	-	ns
Address to data loading time	tADL	200	-	ns
Device resetting time (Read/Program/Erase)	tRST	-	20/30/500	ns
Write protection time	tWW	100	-	ns

Notes:
1. If Reset Command (FFh) is written at Ready state, the device goes into Busy for maximum 5us.
2. Program / Erase Enable Operation: WP high to WE High. Program / Erase Disable Operation: WP Low to WE High.
3. The transition of the corresponding control pins must occur only while WE is held low.
4. tADL is the time from the WE rising edge of final address cycle to the WE rising edge of first data cycle.

2.8. Status Register Coding

Table 2-8. Status Register Coding For 70h/78h command

I/O	Page Program	Block Erase	Read	Cache Read	Cache Program	Coding 70h / 78h
0	Pass / Fail	Pass / Fail	N/A	N/A	Pass / Fail (N)	N page Pass : '0' Fail : '1'
1	N/A	N/A	N/A	N/A	Pass / Fail (N-1)	N-1 page Pass : '0' Fail : '1'
2	N/A	N/A	N/A	N/A	N/A	'0'
3	N/A	N/A	N/A	N/A	N/A	'0'
4	N/A	N/A	N/A	N/A	N/A	'0'
5	N/A	N/A	N/A	Ready / Busy	Ready / Busy	Ready / Busy Busy : '0' Ready : '1'
6	Ready / Busy	Ready / Busy	Ready / Busy	Ready / Busy	Ready / Busy	Data Cache Ready / Busy Busy : '0' Ready : '1'
7	Write Protect	Write Protect	Write Protect	Write Protect	Write Protect	Protected : '0' Not Protected : '1'

Notes:
1. I/O0 : This bit is only valid for Program and Erase operations. During Cache Program operations, this bit is only valid when I/O5

is set to one.

2. I/O1 : This bit is only valid for cache program operations. This bit is not valid until after the second 15h command or the 10h command has been transferred in a Cache program sequence. When Cache program is not supported, this bit is not used.

3. I/O5 : If set to one, then there is no array operation in progress. If cleared to zero, then there is a command being processed (I/O6 is cleared to zero) or an array operation in progress. When overlapped interleaved operations or cache commands are not supported, this bit is not used.

4. I/O6 : If set to one, then the device or interleaved address is ready for another command and all other bits in the status value are valid. If cleared to zero, then the last command issued is not yet complete and Status Register bits<5:0> are invalid value. When cache operations are in use, then this bit indicates whether another command can be accepted, and I/O5 indicates whether the last operation is complete.

Table 2-9. Status Register Coding For 75h command

I/O	Page Program	Block Erase	Read	Cache Read	Cache Program	Coding
						75h
0	/ Fail	/ Fail	N/A	N/A	Chip Pass / Fail (N)	N page Pass : '0' Fail : '1'
1	Plane 0 Pass / Fail	Plane 0 Pass / Fail	N/A	N/A	Plane 0 Pass / Fail (N)	N page Pass : '0' Fail : '1'
2	Plane 1 Pass / Fail	Plane 1 Pass / Fail	N/A	N/A	Plane 1 Pass / Fail (N)	N page Pass : '0' Fail : '1'
3	N/A	N/A	N/A	N/A	Plane 0 Pass / Fail (N-1)	N-1 page Pass : '0' Fail : '1'
4	N/A	N/A	N/A	N/A	Plane 1 Pass / Fail (N-1)	N-1 page Pass : '0' Fail : '1'
5	N/A	N/A	N/A	Ready / Busy	Ready / Busy	Ready / Busy Busy : '0' Ready : '1'
6	Ready / Busy	Ready / Busy	Ready / Busy	Ready / Busy	Ready / Busy	Data Cache Ready / Busy Busy : '0' Ready : '1'
7	Write Protect	Write Protect	Write Protect	Write Protect	Write Protect	Protected : '0' Not Protected : '1'

2.9. Device Identifier Coding

Table 2-10. Product Read ID

	Description
1st Byte	Maker Code
2nd Byte	Device Code

	Description
3rd Byte	Internal Number, Cell Type, Number of Program pages
4th Byte	Page size (without Spare area), Block size (without Additional Block), Redundant Area size
5th Byte	Plane Number, ECC Level
6th Byte	NAND Technology, Interface

Device	1st Cycle	2nd Cycle	3rd Cycle	4th Cycle	5th Cycle	6th Cycle
H27UCG8T2ETR	ADh	DEh	94h	A7h	42h	48h
H27UDG8U2ETR (TBD)		3Ah	95h		44h	

3. Application notes and comments

3.1. System Bad Block Replacement

Devices with Bad Blocks have the same quality level and the same AC and DC characteristics as devices where all the blocks are valid. A Bad Block does not affect the performance of valid blocks because it is isolated from the bit line and common source line by a select transistor. The devices are supplied with all the locations inside valid blocks erased (FFh). The Bad Block Information is written prior to shipping. Any block where the 1st Byte in the spare area of the first and last page does not contain FFh is a Bad Block. The Bad Block Information must be read before any erase is attempted as the Bad Block Information may be erased. For the system to be able to recognize the Bad Blocks based on the original information it is recommended to create a Bad Block table following the flowchart shown in Figure of *"Bad block management flow chart"*. The 1st block, which is placed on 00h block address, is guaranteed to be a valid block at the time of shipment.

Figure 3-1. Bad block management flow chart
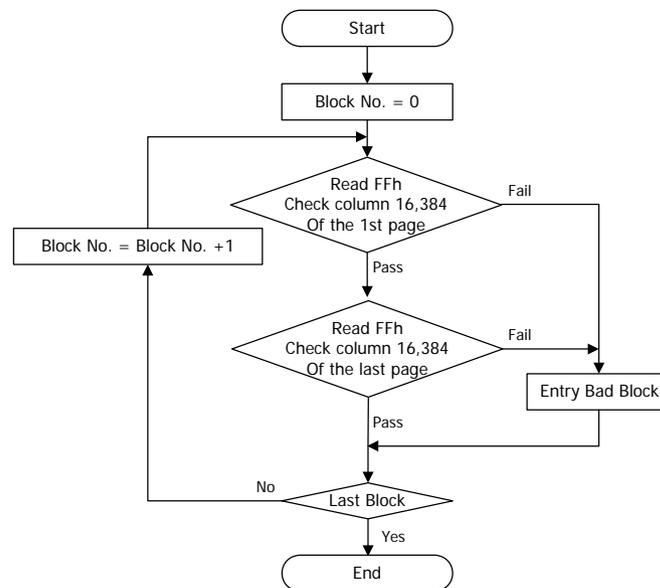
Notes:
1. Do not try to erase the detected bad blocks, because the bad bock information will be lost.
2. Do not perform program and erase operation in invalid block, it is impossible to guarantee the input data and to ensure that the function is normal.

3.2. Bad Block Replacement

This device may have the invalid blocks when shipped from factory. An invalid block is one that contains one or more bad bits. Over the lifetime of the device additional Bad Blocks may develop. In this case, the block has to be replaced by copying the data to a valid block. These additional Bad Blocks can be identified as attempts to program or erase them will give errors in the Status Register.

The failure of a page program operation does not affect the data in other pages in the same block. Bad block can be replaced by re-programming the current data and copying the rest of the replaced block to an available valid block. Refer to Table for "*Block failure*" and Figure of "*Block replacement*" for the recommended procedure to follow if an error occurs during an operation.

Table 3-1. Block failure

Operation	Recommended Procedure
Erase	Block Replacement
Program	Block Replacement
Read	ECC

Figure 3-2. Block replacement

Buffer memory of the controller
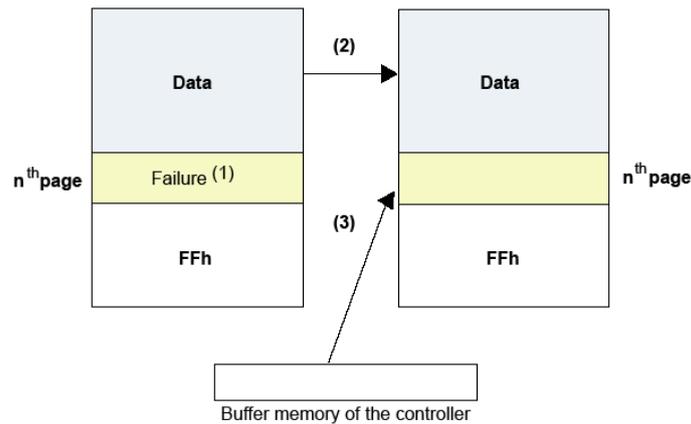
Notes:
1. An error occurs on nth page of the Block A during Program or Erase operation.
2. Data in Block A is copied to same location in Block B which is valid block.
3. Nth page of block A which is in controller buffer memory is copied into nth page of Block B
4. Bad block table should be updated to prevent from erasing or programming Block A.

3.3. Paired page address information

When program operation is abnormally aborted (ex. sudden power-off, reset), not only page data under program but also a cou-pled row paired page data may be corrupted. For example, during page program operation of page address 05h is aborted by reset or power down, the data of 01h and 05h page address may be spoiled.

Table 3-2. Paired Page Address Information

Paired Page Address(1/4)		Paired Page Address(2/4)		Paired Page Address(3/4)		Paired Page Address(4/4)	
Group A	Group B	Group A	Group B	Group A	Group B	Group A	Group B
00h	02h	41h	44h	83h	86h	C5h	C8h
01h	04h	43h	46h	85h	88h	C7h	CAh
03h	06h	45h	48h	87h	8Ah	C9h	CCh
05h	08h	47h	4Ah	89h	8Ch	CBh	CEh
07h	0Ah	49h	4Ch	8Bh	8Eh	CDh	D0h
09h	0Ch	4Bh	4Eh	8Dh	90h	CFh	D2h
0Bh	0Eh	4Dh	50h	8Fh	92h	D1h	D4h
0Dh	10h	4Fh	52h	91h	94h	D3h	D6h
0Fh	12h	51h	54h	93h	96h	D5h	D8h
11h	14h	53h	56h	95h	98h	D7h	DAh
13h	16h	55h	58h	97h	9Ah	D9h	DCh
15h	18h	57h	5Ah	99h	9Ch	DBh	DEh
17h	1Ah	59h	5Ch	9Bh	9Eh	DDh	E0h
19h	1Ch	5Bh	5Eh	9Dh	A0h	DFh	E2h
1Bh	1Eh	5Dh	60h	9Fh	A2h	E1h	E4h
1Dh	20h	5Fh	62h	A1h	A4h	E3h	E6h
1Fh	22h	61h	64h	A3h	A6h	E5h	E8h
21h	24h	63h	66h	A5h	A8h	E7h	EAh
23h	26h	65h	68h	A7h	AAh	E9h	ECh
25h	28h	67h	6Ah	A9h	ACh	EBh	EEh
27h	2Ah	69h	6Ch	ABh	AEh	EDh	F0h
29h	2Ch	6Bh	6Eh	ADh	B0h	EFh	F2h
2Bh	2Eh	6Dh	70h	AFh	B2h	F1h	F4h
2Dh	30h	6Fh	72h	B1h	B4h	F3h	F6h
2Fh	32h	71h	74h	B3h	B6h	F5h	F8h
31h	34h	73h	76h	B5h	B8h	F7h	FAh
33h	36h	75h	78h	B7h	BAh	F9h	FCh
35h	38h	77h	7Ah	B9h	BCh	FBh	FEh
37h	3Ah	79h	7Ch	BBh	BEh	FDh	FFh
39h	3Ch	7Bh	7Eh	BDh	C0h		
3Bh	3Eh	7Dh	80h	BFh	C2h		
3Dh	40h	7Fh	82h	C1h	C4h	-	
3Fh	42h	81h	84h	C3h	C6h		

4. Device Operation

4.1. Page Read

This operation is initialized by 00h-30h to the command register along with followed by five address input cycles.
The 18,048 bytes of data within the selected page are transferred to the data registers in less than tR. The system controller may detect the completion of this data transfer tR by analyzing the output of R/B pin. Once the data in a page is loaded into the data registers, they may be read out in 20ns cycle time by sequentially pulsing RE#. The repetitive high to low transitions of the RE clock make the device output the data starting from the selected column address up to the last column address.

The device may output random data in a page instead of the consecutive sequential data by writing random data output command. The column address of next data, which is going to be out, may be changed to the address, which follows random data output command. Random data output can be operated multiple times, regardless of how many times it is done in a page.

Figure 4-1. Page read
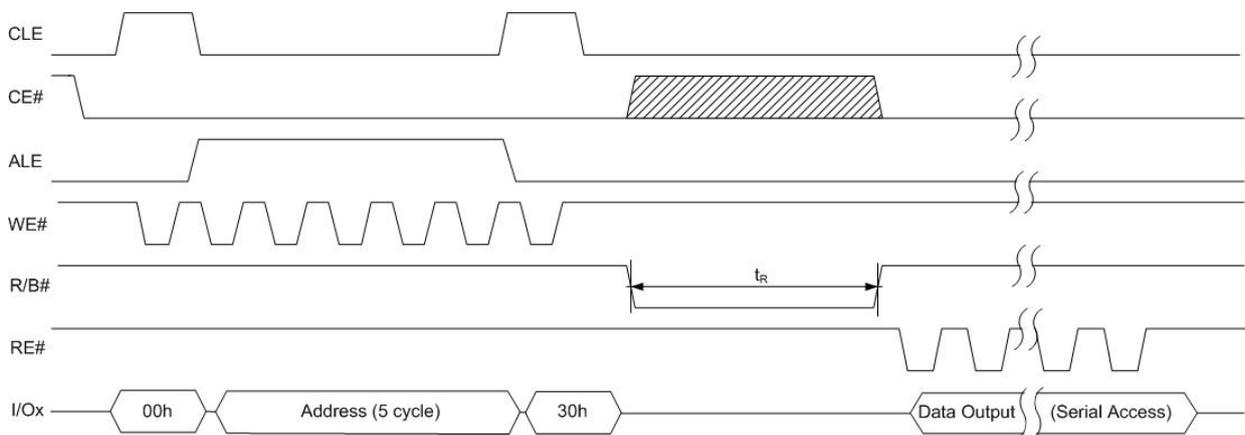
Random data output
Random data output operation changes the column address from which data is being read in the page register.
Random data output only is issued in Ready state. Refer to Figure of "*Random data output*".

Figure 4-2. Random data output
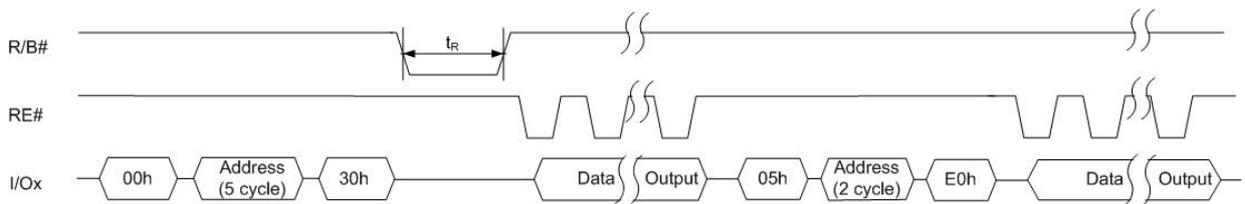
4.2. Cache Read

To improve page read throughput, cache read operation is used within a block. First step is same as normal page read, issuing a page read sequence (00-30h). After random access (R/B returns to high), 31h command is latched into the command register. Data is being transferred from the data register to the cache register. While cache register data is outputted, next page is transferred from memory cell to data register. R/B will stay low during present page random accessing and previous page transferring to cache register. Because it is not necessary to output a whole page data before issuing another 31h command, if serial data output time exceeds random access time (tR), the random access time can be hidden. The subsequent pages are issued additional 31h commands. To terminate cache read, 3Fh command should be issued. This command transfer data from data register to the

cache register without issuing next page read. During the Cache Read Operation, device doesn't allow any other command except Cache Read command (31h), Read Status (70h, 78h, 75h), Read (00h), and Reset (FFh). To carry out other operations after cache operation, cache read must be ended by 3Fh command or issue reset (FFh) before next operation.

Figure 4-3. Cache read
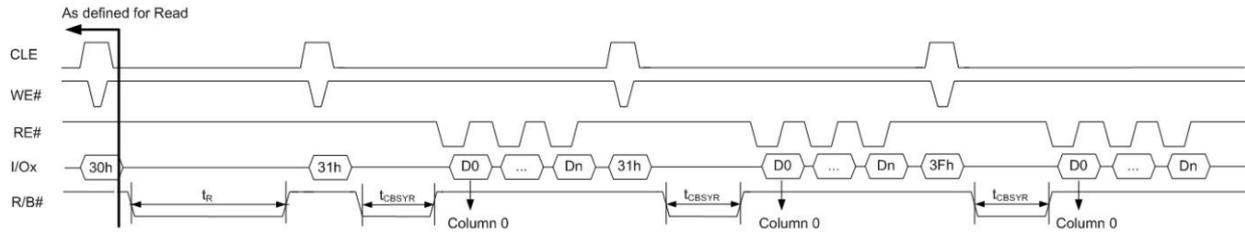
4.3. Cache Read Enhanced (available only within a block)

This command extends the Cache Read command. While, by issuing a Cache Read command, the next page address of the next page is automatically incremented by 1, the next page address of the next page is given arbitrarily by the user. The Cache Read Enhanced command sequence consists of a 00h command, five address cycles and a 31h command, which replaces the single 31h command of the Cache Read command sequence.

4.4. Multi Plane Page Read

Multi-Plane Page Read is an extension of Page Read, for a single plane with 18,048byte page registers. Since the device is equipped with two memory planes, activating the two sets of 18,048byte page resisters enables a random read of two pages. Multi-Plane Page Read is initiated by repeating command 60h followed by three address cycles twice. In this case, only same page of each block can be selected from each plane.

After Read Confirm command (30h) the 18,048bytes of data within the selected two pages are transferred to the data registers in less than t_R. The system controller can detect the completion of data transfer (t_R) by monitoring the output of R/$\overline{B}$ pin.

Once the data is loaded into the data registers, the data output of first plane can be read out by issuing command 00h with Five Address Cycles, command 05h with two column address and finally E0h. The data output of second plane can be read out using the identical command sequences. The restrictions for Multi-Plane Page Read are shown in Figure of "*Multi plane page read*". Multi-Plane Page Read must be used in the block which has been programmed with Multi-Plane Page Program.

Figure 4-4. Multi plane page read
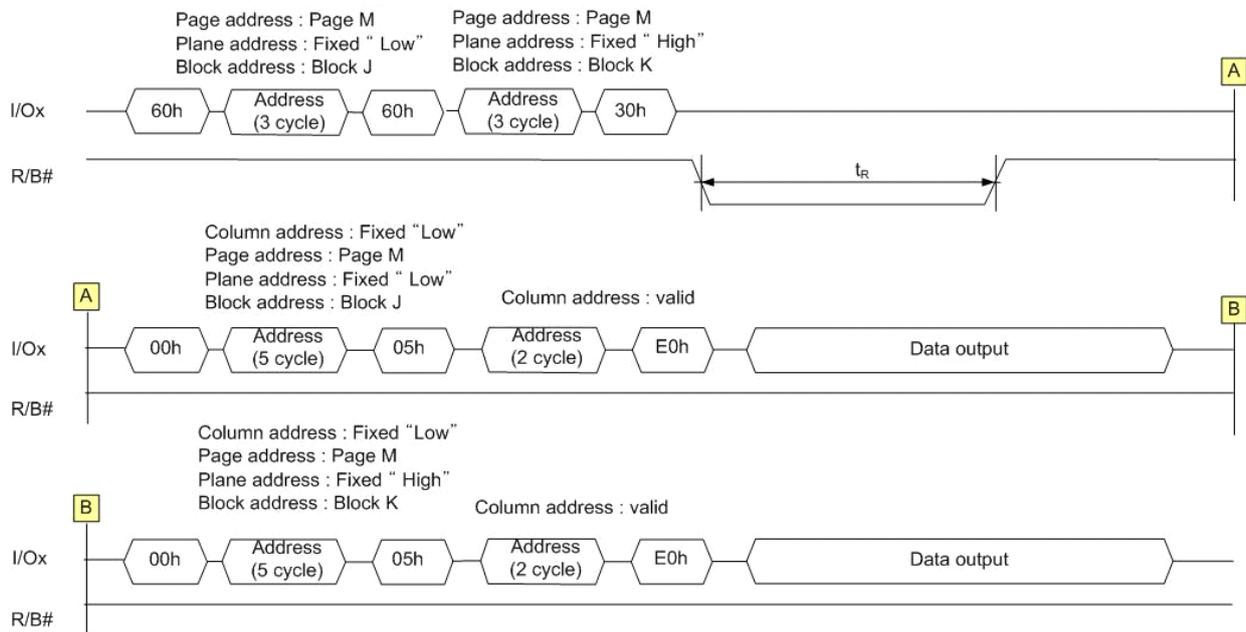
4.5. Multi Plane Cache Read (available only within a block)

The device supports multi-plane cache read, which enables high read throughput by reading two pages in parallel. Figure of "*Multi plane cache read*" shows the command sequence for the multi-plane cache read operation. Both confirm commands, 30h and 33h, are valid for the first page read sequence.

Figure 4-5. Multi plane cache read
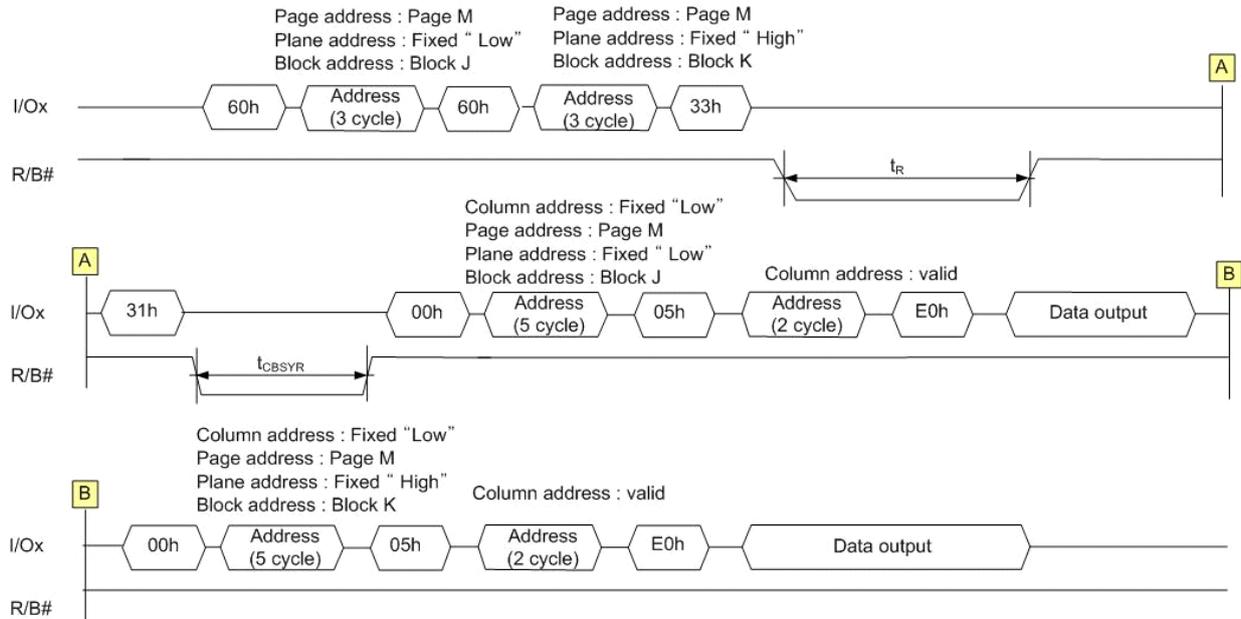
Notes:
1. plane 0 and plane 1 should be selected within the same chip
2. Only one block should be selected from the each plane.
3. Multi plane cache read is available only within a block per plane.
4. Selected Page address except A23 within two blocks must be same.
5. The operation has to be terminated with "3Fh" command.
6. It's possible to confirm the multi-plane cache read first step using both 30h and 33h.

4.6. Multi Plane Cache Read Enhanced (available only within a block)

This command is a multi-plane extension of the Cache Read Enhanced command.

4.7. Read ID

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. Six read cycles sequentially output the manufacturer code (ADh), and the device code and 3rd, 4th, 5th, 6th cycle ID, respectively. The command register remains in Read ID mode until further commands are issued to it. Figure of "*Read ID*" shows

the operation sequence, while table of "2-10 *Product Read ID*" explain the byte meaning.

Figure 4-6. Read ID
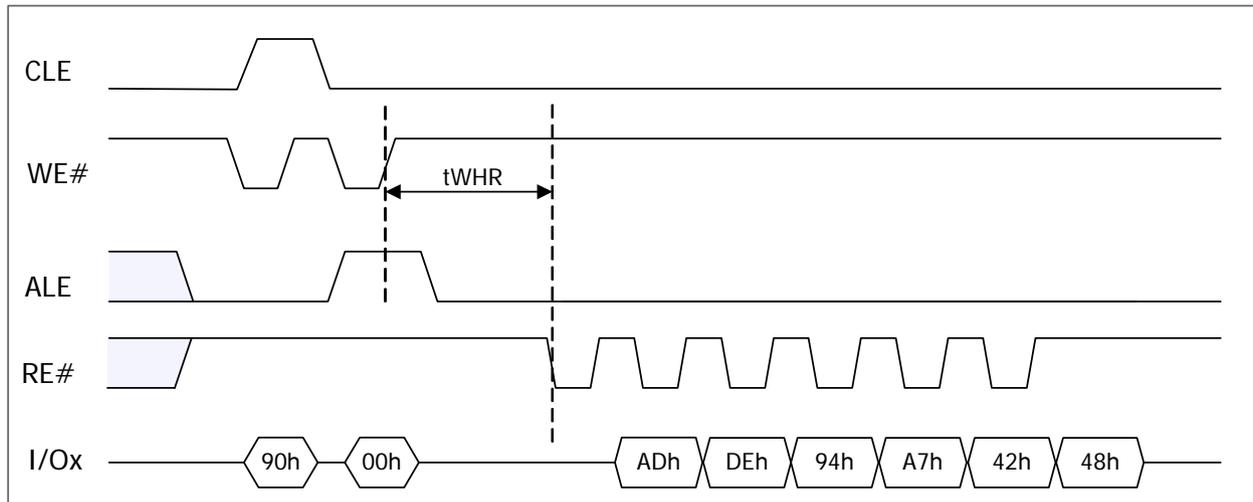
4.8. Read Status Register

The device contains a Status Register which may be read to find out whether read, program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing Read Status (70h) or Multi Plane Read Status (78h,75h) command to the command register, a read cycle outputs the content of the Status Register to the I/O pins only if CE and RE are low, whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when R/B pins are common-wired. Refer to "2.8. STATUS REGISTER CODING" for specific Status Register definitions and Figure of "*Read status*", Figure "*Multi plane read status*" for Read Status. The command register remains in Read Status mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, the read command (00h) should be given before starting read cycles.

Figure 4-7. Read status
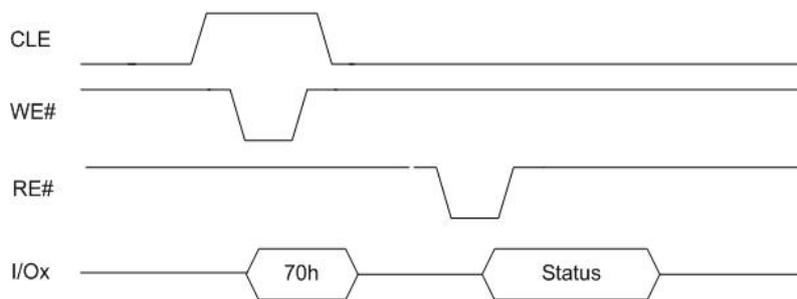
Figure 4-8. Multi plane read status
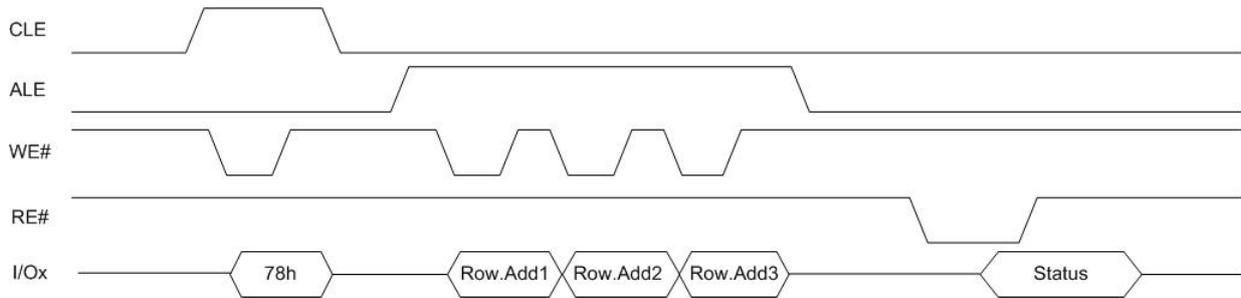
4.9. Page Program

The device is programmed as a page unit. The number of consecutive partial page programming operation within the same page without an intervening erase operation must not exceed 1 times. The program addressing should be done in sequential order in a block. A page program cycle consists of a serial data loading period in which up to 18,048 bytes of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. The serial data-loading period begins by inputting the Serial Data Input command (80h), followed by the five cycle address inputs and then serial data.

The words other than those to be programmed do not need to be loaded. The device supports random data input in a page. The column address of next data, which will be entered, may be changed to the address which follows random data input command (85h). Random data input may be operated multiple times, regardless of how many times it is done in a page. The Page Program Confirm command (10h) initiates the programming process. Writing 10h alone without previously entering the serial data will not initiate the programming process.

The internal write state controller automatically executes the algorithms and timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be entered to read the status register.

The system controller can detect the completion of a program cycle by monitoring the R/B̄ output, or the Status bit (I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. The Write Status Bit (I/O 0) is valid, when all internal operations are complete (status bit I/O 6 = high).
The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s.
The command register remains in Read Status command mode until another valid command is written to the command register.
Figure of "*Page Program*" and Figure of "*Random data input*" details the sequence.

Figure 4-9. Page Program
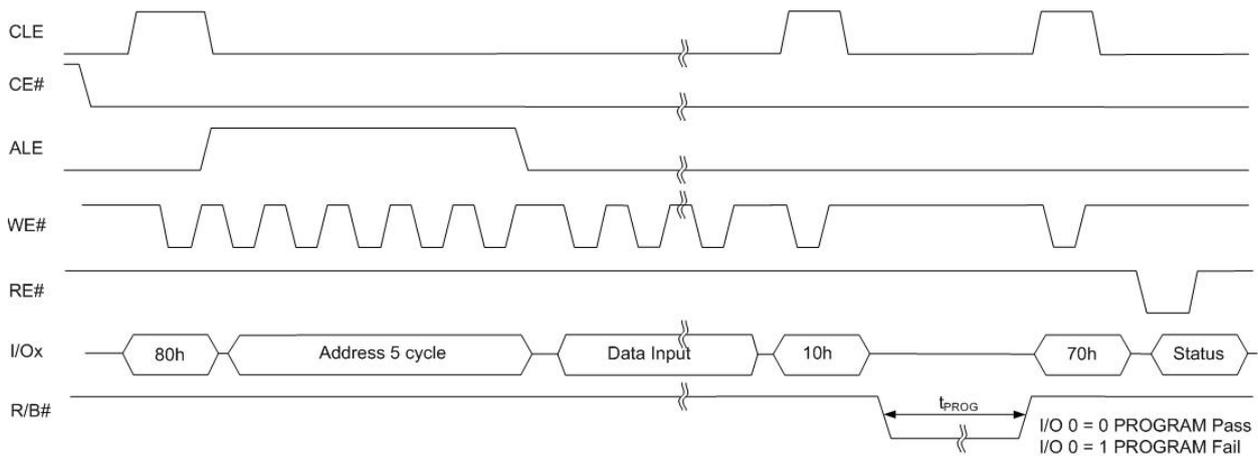
Figure 4-10. Random data input
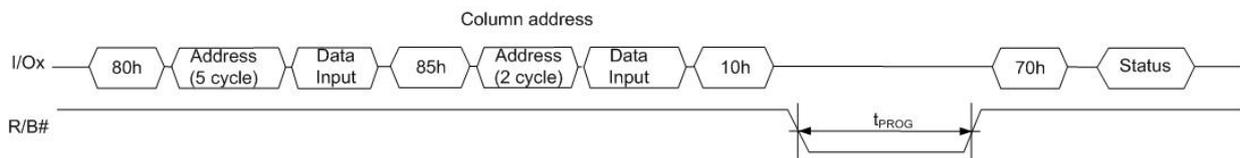
4.10. Multi Plane Program

Device supports multiple plane program. It is possible to program in parallel 2 pages, one per each plane.
A multiple plane program cycle consists of a double serial data loading period in which up to 18,048bytes of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. The serial data loading period begins by inputting the Serial Data Input command (80h), followed by the five cycle address inputs and then serial data for the 1st page. Address for this page must be within first plane (A<23>=0). The data of first page other than those to be programmed do not need to be loaded. The device supports random data input exactly like page program operation. The Dummy Page Program Confirm command (11h) stops 1st page data input and the device becomes busy for a short time (tDBSY).

Once it has become ready again, 81h command must be issued, followed by second page address (5 cycles) and its serial data input. Address for this page must be within second plane (A<23>=1). The data of second page other than those to be programmed do not need to be loaded. Program Confirm command (10h) makes parallel programming of both pages start. User can check operation status by R/B pin or read status register command, as if it were a normal page program; status register command is also available during Dummy Busy time (tDBSY). In case of fail in first plane or second plane page program, fail bit of status register will be set:
Pass/Fail status of each plane can be checked by Multi Plane Read Status. Figure of "*Multi plane page program*" details the sequence.

Figure 4-11. Multi plane page program
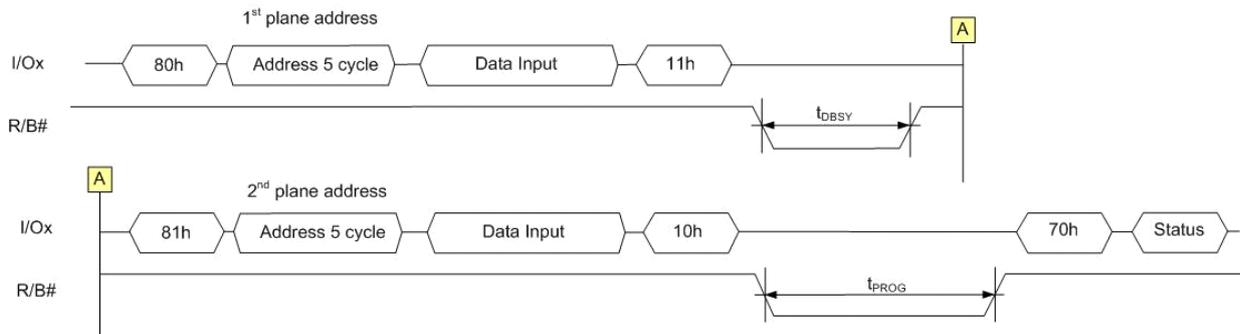
Notes:
1. plane 0 and plane 1 should be selected within the same chip.
2. Only one block should be selected from the each plane.
3. Selected Page address except A23 within two blocks must be same.
4. Any command between 11h and 81h is prohibited except 70h/78h/75h and FFh.
5. Read Status command can be 70h or 78h or 75h.

4.11. Cache Program (available only within a block)

Cache Program is an extension of the standard page program, which is executed with 18,048 bytes cache registers and same bytes data register. After the serial data input command (80h) is loaded to the command register, followed by 5 cycles of address, a full or partial page of data is latched into the cache register, and then the cache write command (15h) is loaded to the command register. After that sequence, the data in the cache register is transferred into the data register for cell programming. At this time, the device remains in busy state. After all data of the cache register is transferred into the data register, the device goes to the Ready state to load the next data into the cache register by issuing another cache program command sequence (80h-15h).

There are some restrictions for cache program operation.
1. The cache program command is available only within a block.
2. User must give address and data after 80h command.

The Busy time of first sequence equals the time it takes to transfer the data of cache register to the data register.
Cell programming of the data of data register and loading of the next data into the cache register is consequently processed as a pipeline method. On the second and cascading sequence, transfer from the cache register to the data register is held off until cell programming of current data register contents has been done.
Read Status command (70h) may be issued to find out when the cache register is ready by polling the Cache Busy status bit (I/O 6). In addition, the status bit (I/O 5) can be used to determine when the cell programming of the current data register contents is complete. Pass/fail status of only the previous page (I/O 1) is available upon the return to Ready state.

If the system monitors the progress of programming only with R/$\overline{\text{B}}$, the last page of the target programming sequence must be programmed with actual Page Program command (10h). If the Cache Program command (15h) is used instead, status bit (I/O5) must be polled to find out when the last programming is actually finished before starting other operations such as read. Pass/fail status is available in two steps. I/O 1 returns with the status of the previous page upon Ready or I/O6 status bit changing to "1", and later I/O 0 with the status of current page upon true Ready (returning from internal programming) or I/O 5 status bit changing to "1". I/O 1 may be read together when I/O 0 is checked. Refer to "2.8. Status Register Coding" and Figure of "*Cache program*" for more details.

Figure 4-12. Cache program
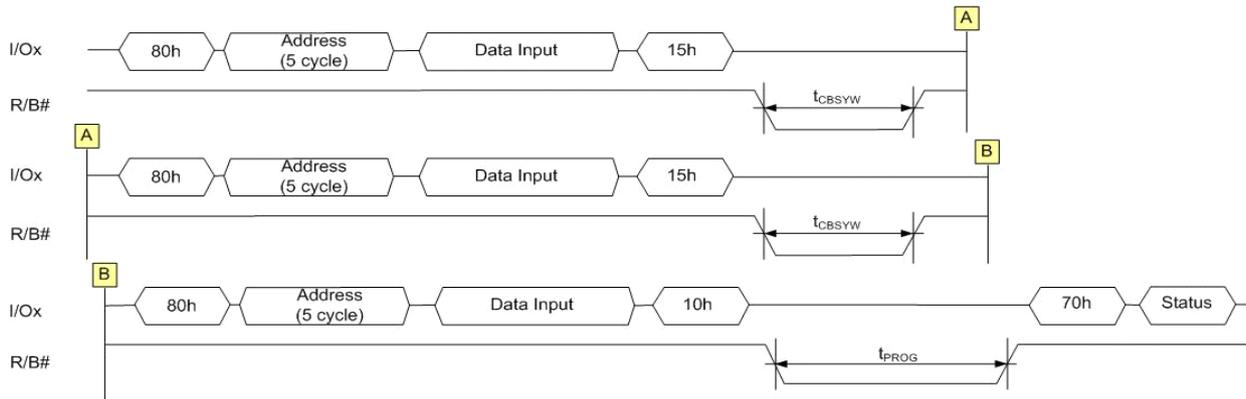
Pass/Fail status for each page programmed by the Cache program operation can be detected by the Read status operation.

■ I/O0 : Pass/Fail of the current page program operation.

■ I/O1 : Pass/Fail of the previous page program operation.

The Pass/Fail status on I/O0 and I/O1 are valid under the following conditions.

■ Status on I/O0 : Ready/Busy is Ready state.

The Ready/Busy is output on I/O5 by Read status operation or $R/\overline{B}$ pin after the 10h command.

■ Status on I/O1 : Data Cache Ready/Busy is Ready state.

The Data Cache Ready/Busy is output on I/O6 by Read status operation or $R/\overline{B}$ pin after the 15h command.

Figure 4-13. Cache Read with Status Read

During both I/O6 and I/O5 return to high, the Pass/Fail for previous page and current page can be shown through I/O1 and I/O0 concurrently.
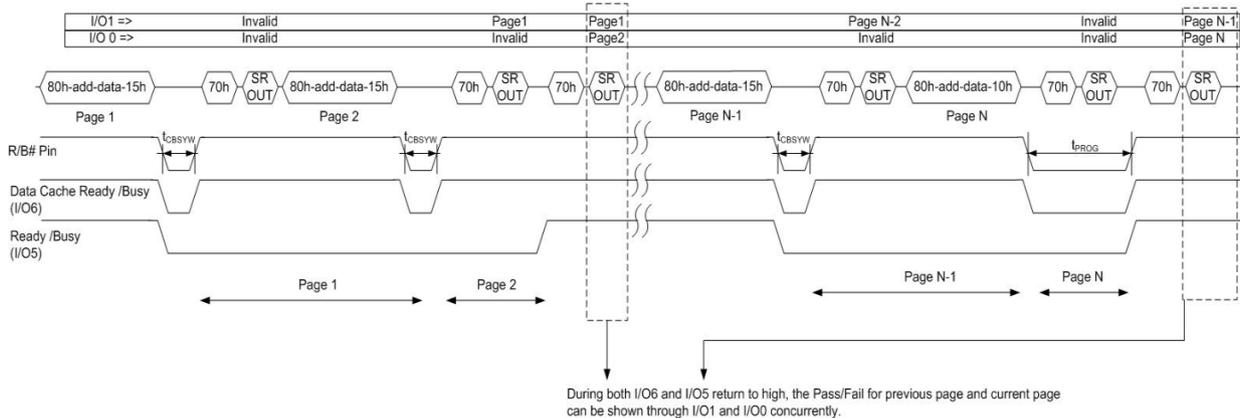
4.12. Multi Plane Cache Program (available only within a block)

The device supports multi-plane cache program, which enables high program throughput by programming two pages. The serial data-loading period begins by inputting the Serial Data Input command (80h), followed by the five cycle address inputs and then serial data for the first page. Address for this page must be within first plane (A<23>=0). The data of first page other than those to be programmed do not need to be loaded. The device supports random data input exactly like page program operation. The Dummy Page Program Confirm command (11h) stops 1st page data input and the device becomes busy for a short time (tDBSY). Once it has become ready again, 81h command must be issued, followed by 2nd page address (5 cycles) and its serial data input. Address for this page must be within second plane (A<23>=1). The data of second page other than those to be programmed do

not need to be loaded. Cache Program Confirm command (15h) makes parallel programming of both pages start. And last page inputs Program confirm command (10h). Figure of "*Multi plane cache program*" shows the command sequence for Multi Plane Cache Program operation. After the "15h" or "10h" command, the result per plane of the operation is shown through the "78h" Multi Plane Read Status command.

Figure 4-14. Multi plane cache program
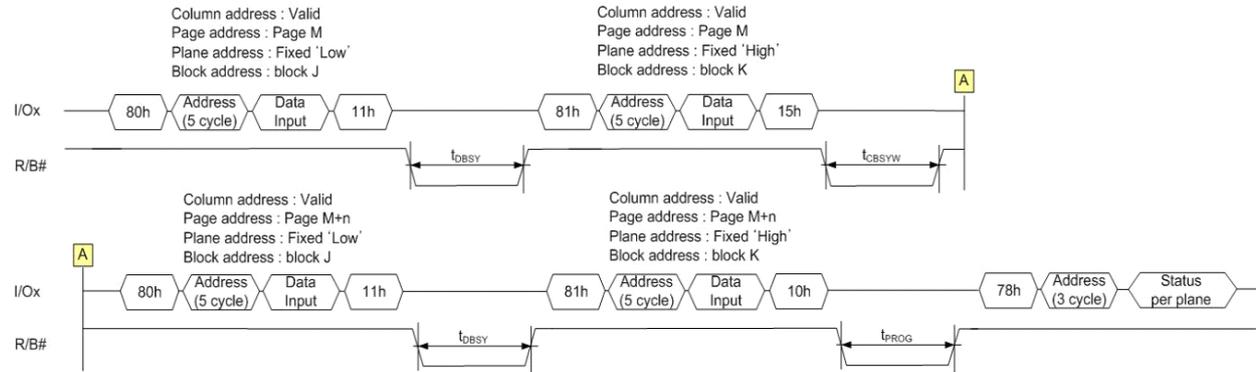
Notes:
1. plane 0 and plane 1 should be selected within the same chip
2. Only one block should be selected from the each plane.
3. Multi plane cache program is available only within a block per plane.
4. Selected Page address except A23 within two blocks must be same.
5. The operation has to be terminated with "10h" command.
6. Any command between 11h and 81h is prohibited except 70h/78h/75h and FFh.
7. Read Status command can be 70h or 78h or 75h. Reading the Status per plane is available only 78h.

4.13. Copy-Back Program

Copy-Back program with Read for Copy-Back is configured to quickly and efficiently rewrite data stored in one page without data reloading when the bit error is not in data stored. Since the time-consuming re-loading cycles are removed, the system perfor-mance is improved. The benefit is especially obvious when a portion of a block is updated and the rest of the block needs to be copied to the newly assigned free block. Copy-Back operation is a sequential execution of Read for Copy-Back and of copy-back program with the destination page address. A read operation with "35h" command and the address of the source page moves the whole 18,048byte data into the internal data buffer. A bit error is checked by sequential reading the data output. In the case where there is no bit error, the data do not need to be reloaded. Therefore, Copy-Back program operation is initiated by issuing Page-Copy Data-Input command (85h) with destination page address. Actual programming operation begins after Program Con-firm command (10h) is issued. Once the program process starts, the Read Status Register command (70h) may be entered to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/B output, or the Sta-tus bit (I/O 6) of the Status Register. When the Copy-Back Program is complete, the Write Status Bit (I/O 0) may be checked. The command register remains in Read Status command mode until another valid command is written to the command register. Dur-ing copy-back program, data modification is possible using random data input command (85h) as shown in Figure of "*Copy-back program*".

Figure 4-15. Copy-back program
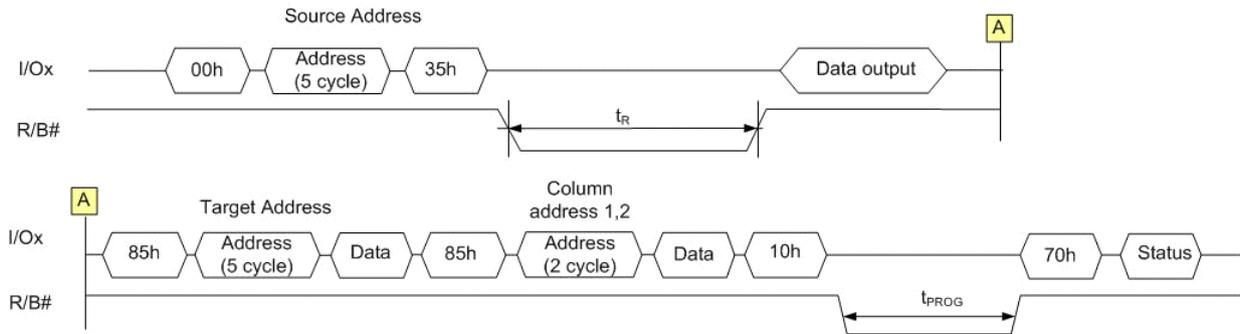
4.14. Multi-Plane Copy-Back Program

Multi-Plane Copy-Back Program is an extension of Copy-Back Program, for a single plane with 18,048 byte page registers. Since the device is equipped with two memory planes, activating the two sets of 18,048 byte page registers enables a simultaneous programming of two pages. Figure of "*Multi plane Copy-back program(I)*" and Figure of "*Multi plane Copy-back program(II)*" show command sequence for the multi-plane copy-back operation. First case, Figure of "*Multi plane Copy-back program(I)*", shows random data input of two planes that started right after finishing random data output of previous two planes. Second case, Figure of "*Multi plane Copy-back program(II)*", shows the random data input of each plane which started right after finishing the random data output of each plane.

Figure 4-16. Multi plane Copy-back program(I)
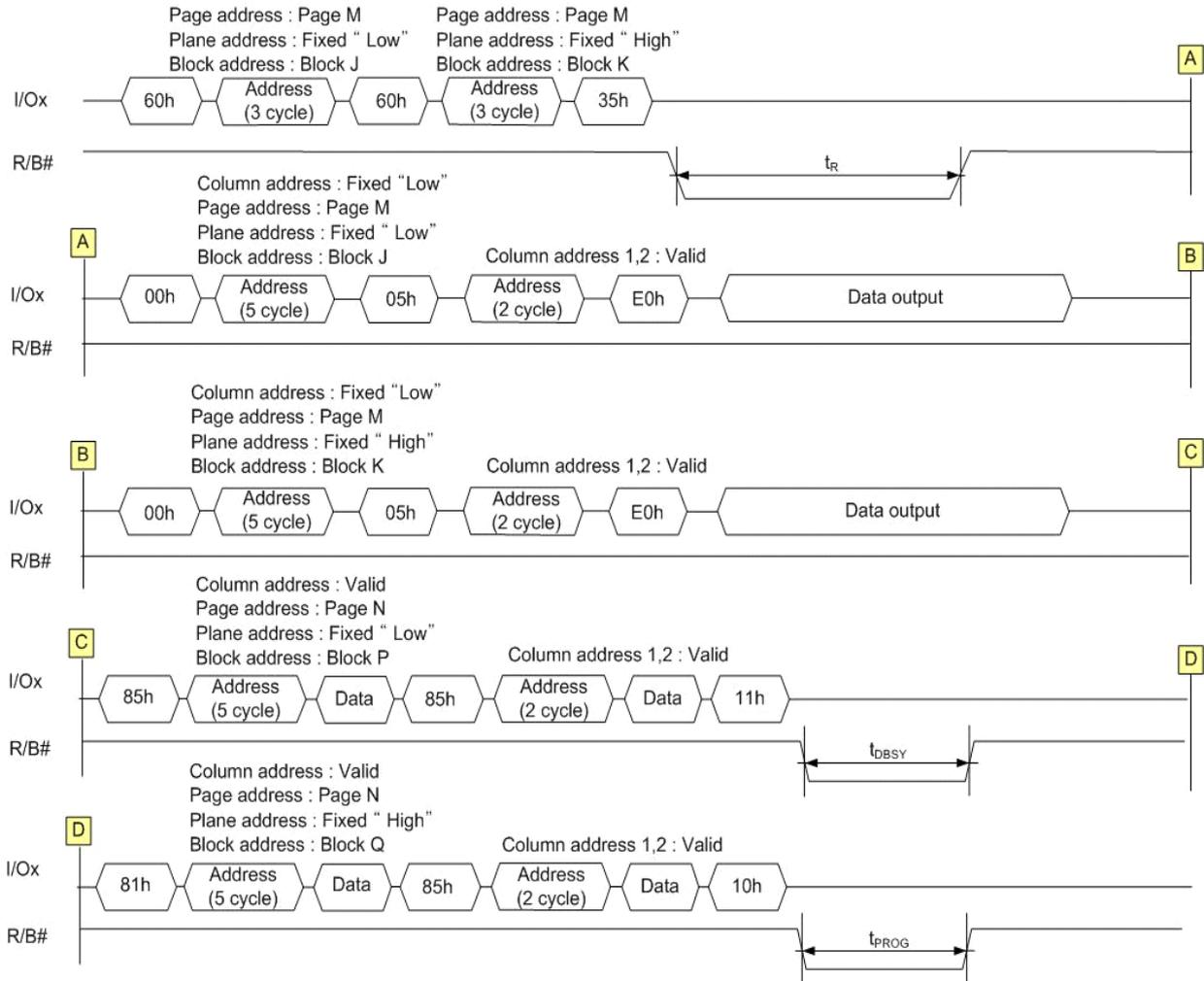
Figure 4-17. Multi plane Copy-back program (II)
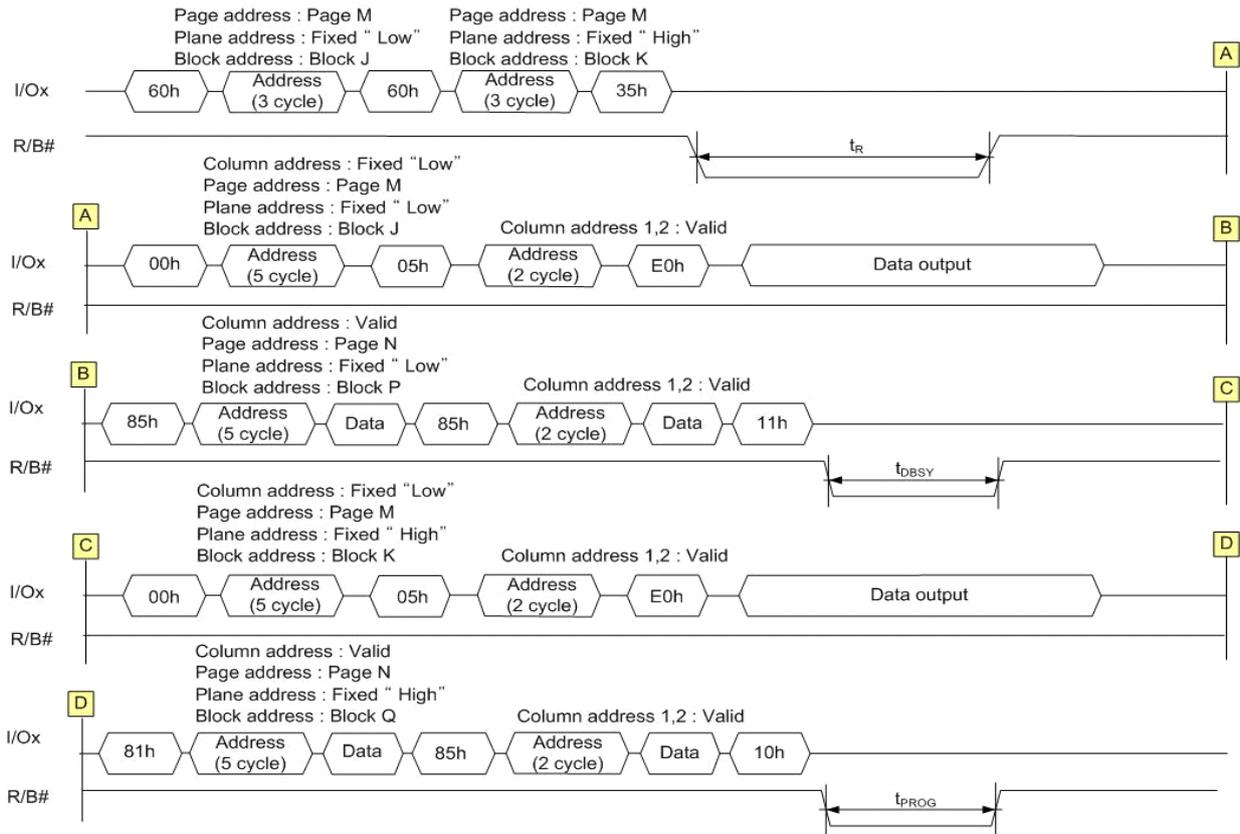
4.15. Block Erase

The Erase operation is done on a block basis. Block address loading is accomplished in two cycles initiated by an Erase Setup command (60h). Only address A24 to A34 is valid while A15 to A22 is ignored. The Erase Confirm command (D0h) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions.

At the rising edge of $\overline{WE}$ after the erase confirm command input, the internal write controller handles erase and erase verify. Once the erase process starts, the Read Status Register command may be entered to read the status register.
The system controller can detect the completion of an erase by monitoring the R/B# output, or the Status bit (I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while erasing is in progress. When the erase operation is completed, the Write Status Bit (I/O 0) may be checked.

Figure 4-18. Block Erase
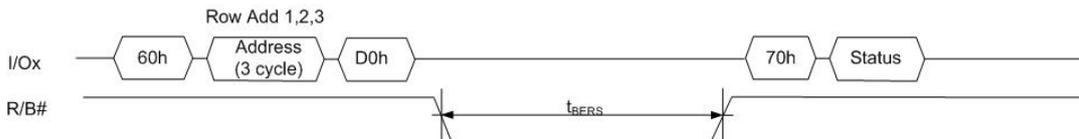
4.16. Multi Plane Block Erase

Multiple plane erase, allows parallel erase of two blocks, one per each memory plane.
Block erase setup command (60h) must be repeated two times, each time followed by first block and second block address respectively (3 cycles each). As for block erase, D0h command makes embedded operation start. Multi plane erase does not need any Dummy Busy Time between first and second block address insertion. Address limitation required for Multiple Plane Program applies also to multiple plane erase, as well as operation progress can be checked like for Multiple Plane Program. Refer to the detail sequence as shown below.

Figure 4-19. Multi plane Block Erase
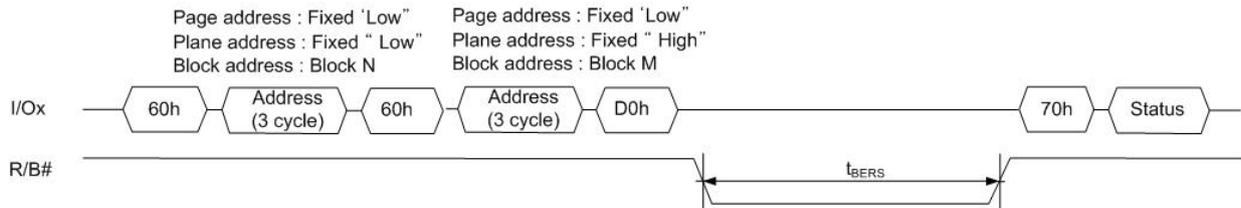
4.17. Reset

The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value E0h when WP is high. Refer to "2.8. Status Register Coding" for device status after reset operation. If the device is already in reset state, the command register will not accept a new reset command. The R/B pin goes low for t_{RST} after the Reset command is written. Refer to Figure of "*Reset*".

Figure 4-20. Reset
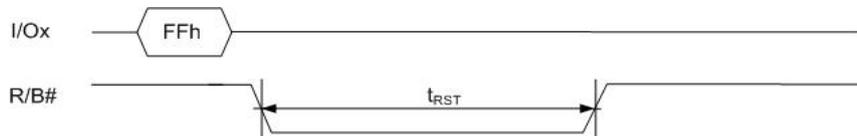
5. Other Features

5.1. Data Protection & Power on/off Sequence

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever VCC is below about 2.0V (3.3V device). WP pin provides hardware protection and is recommended to be kept at V$_{IL}$ during power-up and power-down.

The reset command (FFh) must be issued to all dies as the first command after device is power up. Each R/B will be busy for maximum of 2ms after reset command is issued. In this time, the acceptable command is 70h or 78h or 75h.

Figure 5-1. Data protection and power on / off
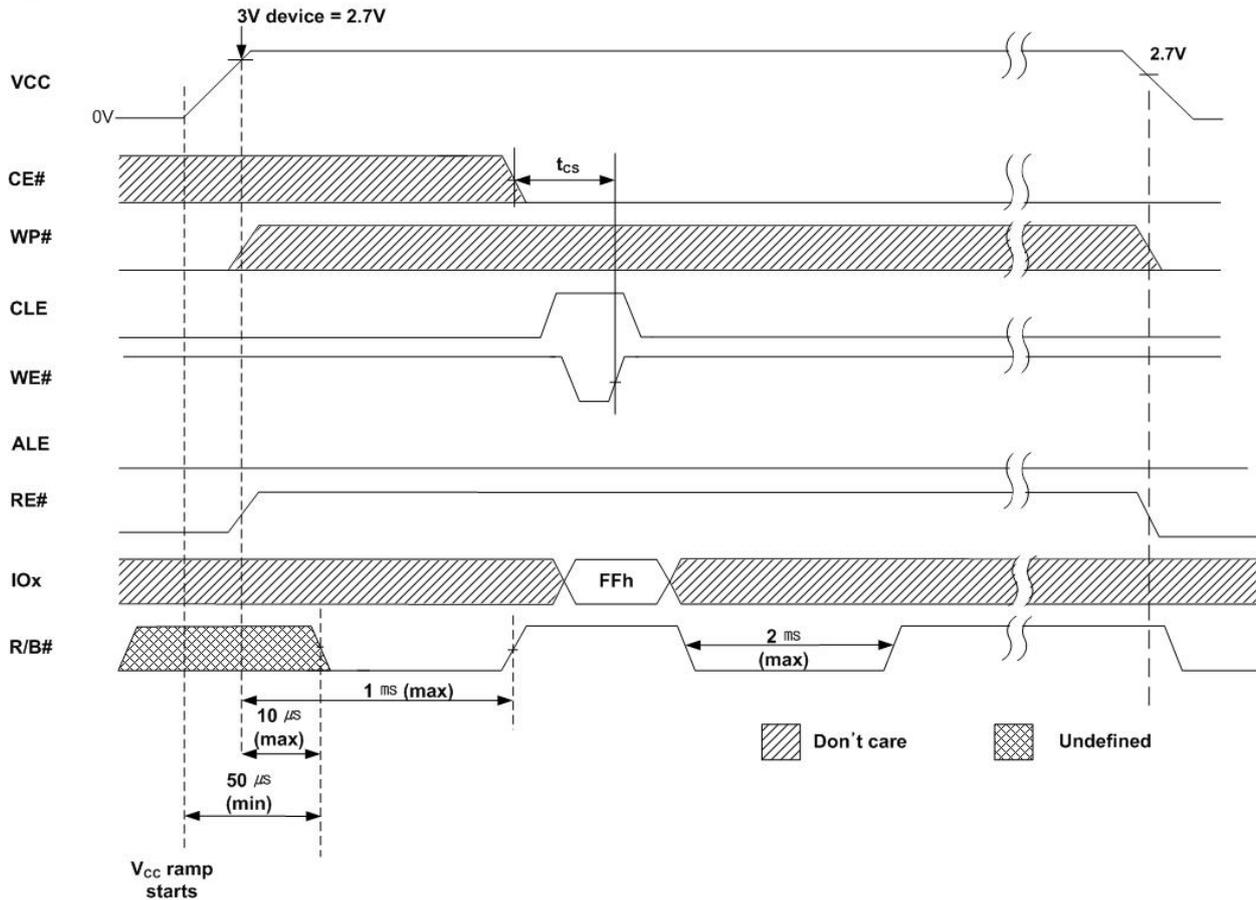
5.2. Ready / Busy

The device has a Ready/Busy output that provides method of indicating the completion of a page program, erase, copy-back and random read completion. The R/B pin is normally high and goes to low when the device is busy (after a reset, read, program, and erase operation). It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/B outputs to be Or-tied. Because pull-up resistor value is related to tR (R/B) and current drain during busy (Ibusy), an appropriate value can be obtained with the following reference chart (Figure of "*Ready / Busy*"). Its value can be determined by the following guidance.

Figure 5-2. Ready / Busy
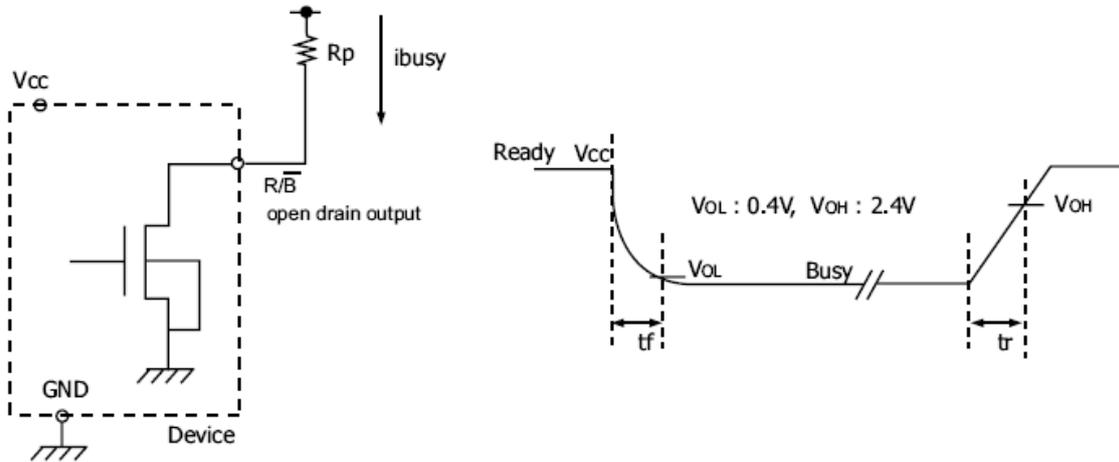
Fig. Rp vs tr, tf & Rp vs ibusy

@ Vcc = 3.3V, Ta = 25°C, C$_L$=50pF
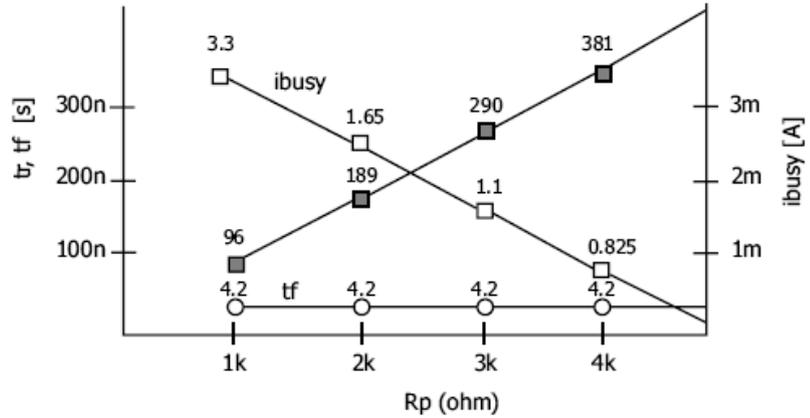
Rp value guidence

$$Rp\ (min) = \frac{Vcc\ (Max.) - V_{OL}\ (Max.)}{I_{OL} + \Sigma I_L} = \frac{3.2V}{8mA + \Sigma I_L}$$

where IL is the sum of the input currnts of all devices tied to the R/B̄ pin.

Rp(max) is determined by maximum permissible limit of tr

5.3. Write Protect Operation

The Erase and Program Operations are automatically reset when $\overline{WP}$ goes Low (tWW = 100ns, min). The operations are enabled and disabled as follows.

Figure 5-3. Enable Programming / Disable Programming
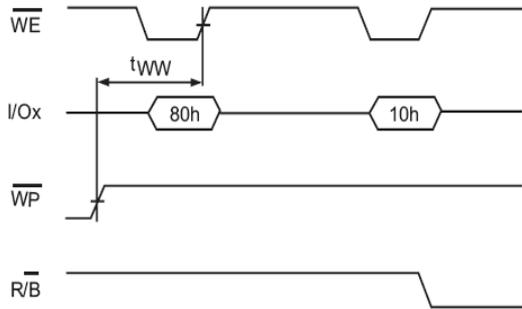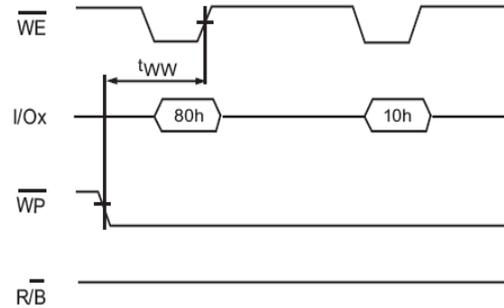
Figure 5-4. Enable Erasing / Disable Erasing
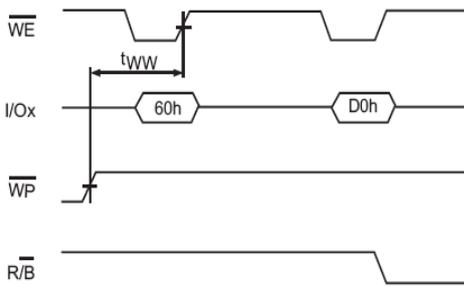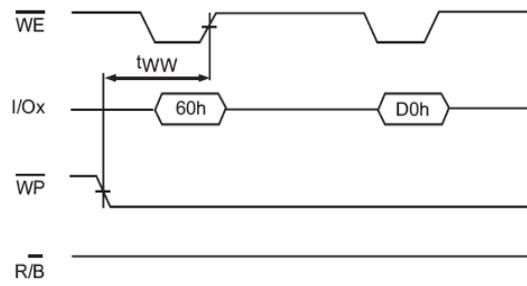
7. Timing Diagram

Figure 1. Command Latch Cycle Timings
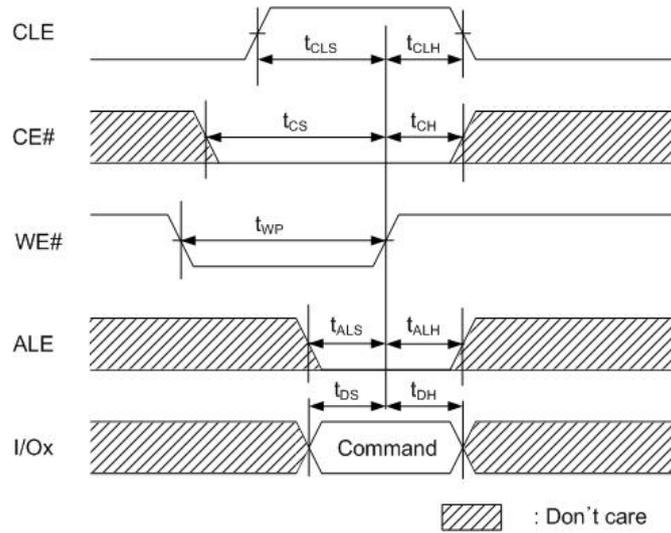
Figure 2. Address Latch Cycle Timings
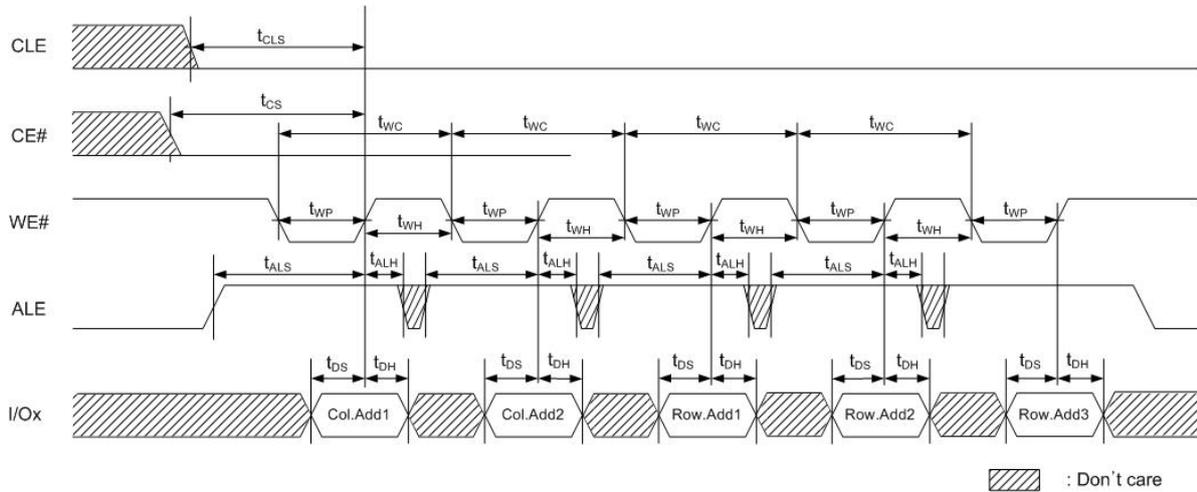
Figure 3. Input Data Latch Cycle Timings
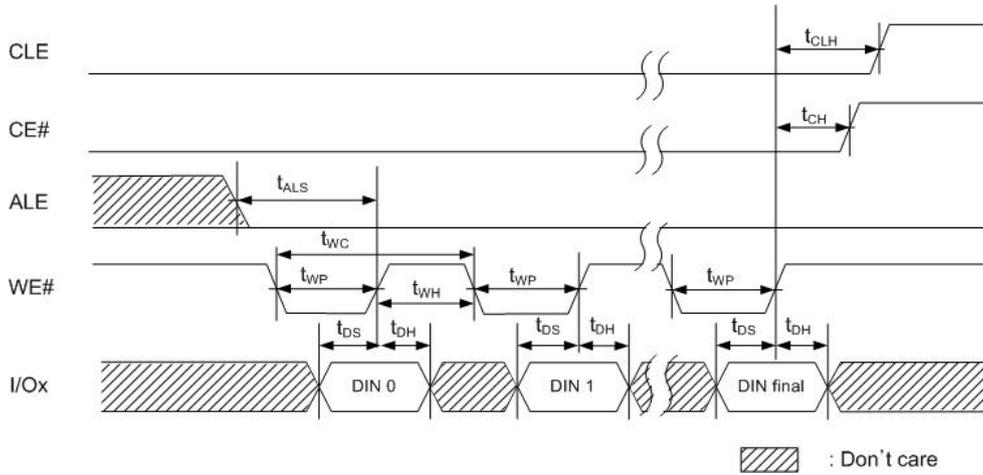
Figure 4. Data Output Cycle Timings (CLE=L, $\overline{WE}$=H, ALE=L, $\overline{WP}$=H)
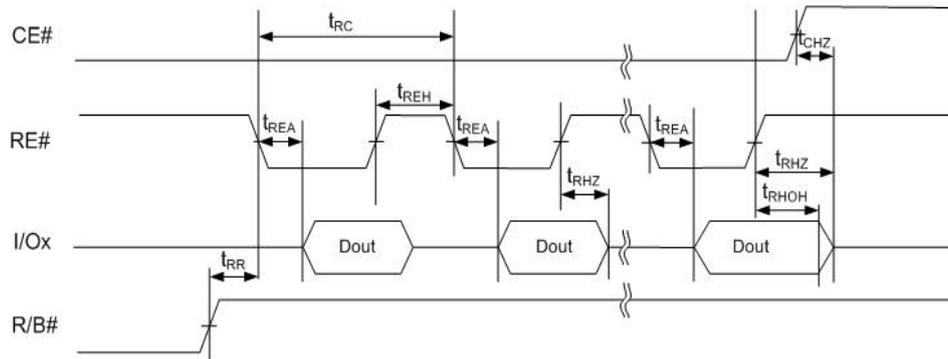
Figure 5. Data Output Cycle Timings (EDO type, CLE=L, $\overline{WE}$=H, ALE=L)
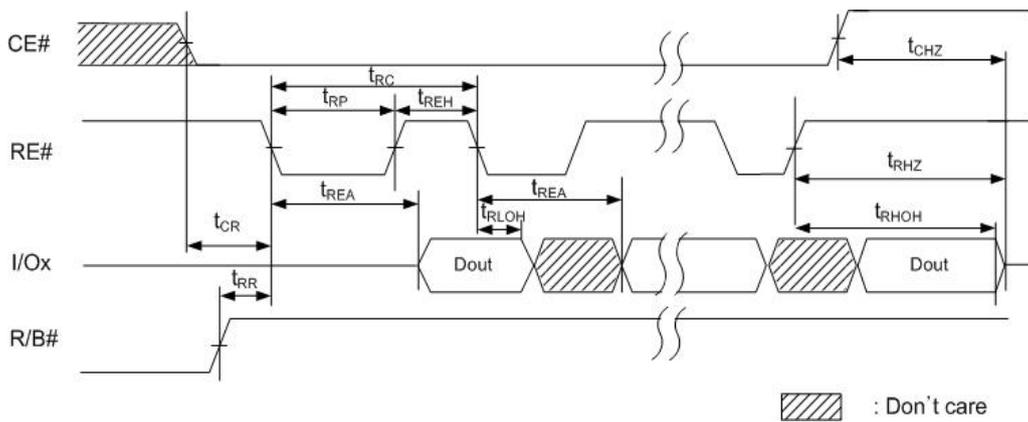
Figure 6. Read Status Cycle Timings
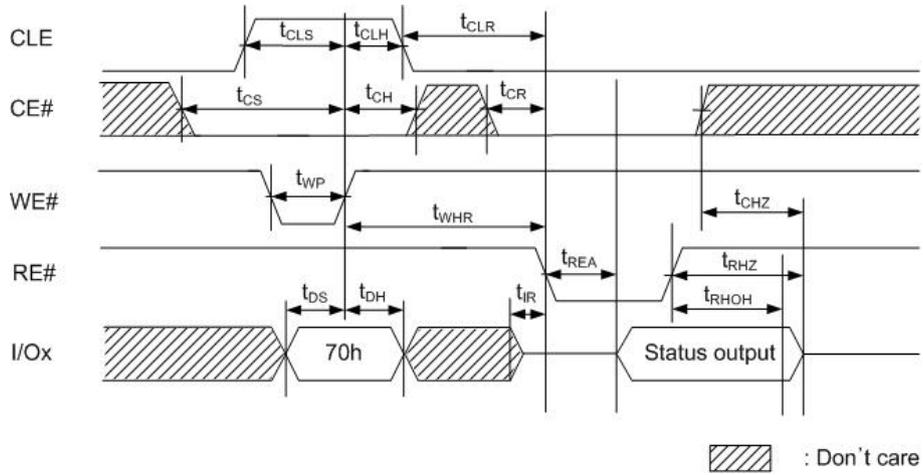
Figure 7. Multi-Plane Read Status Timings
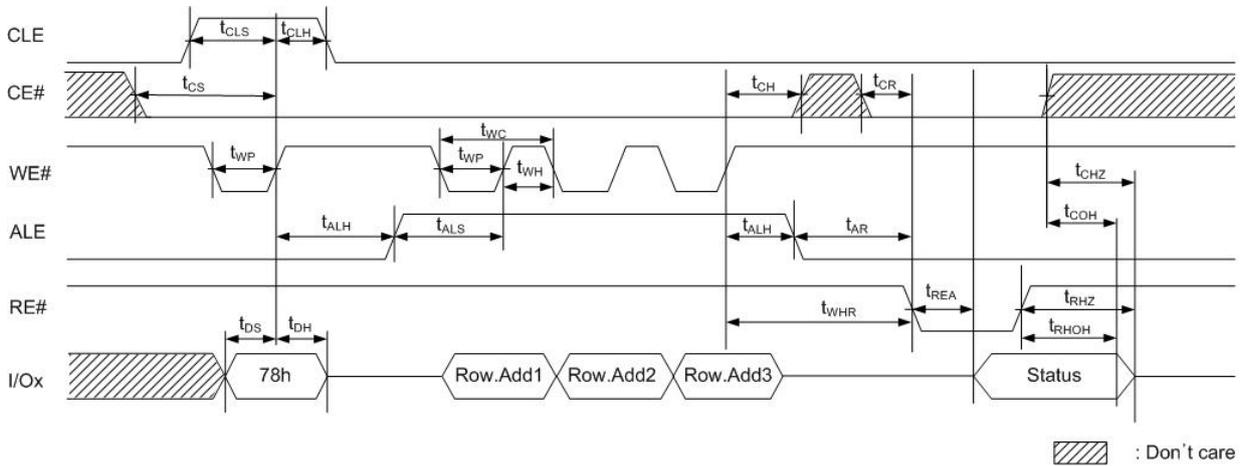
Figure 8. Page Read Operation Timings (Read One Page)
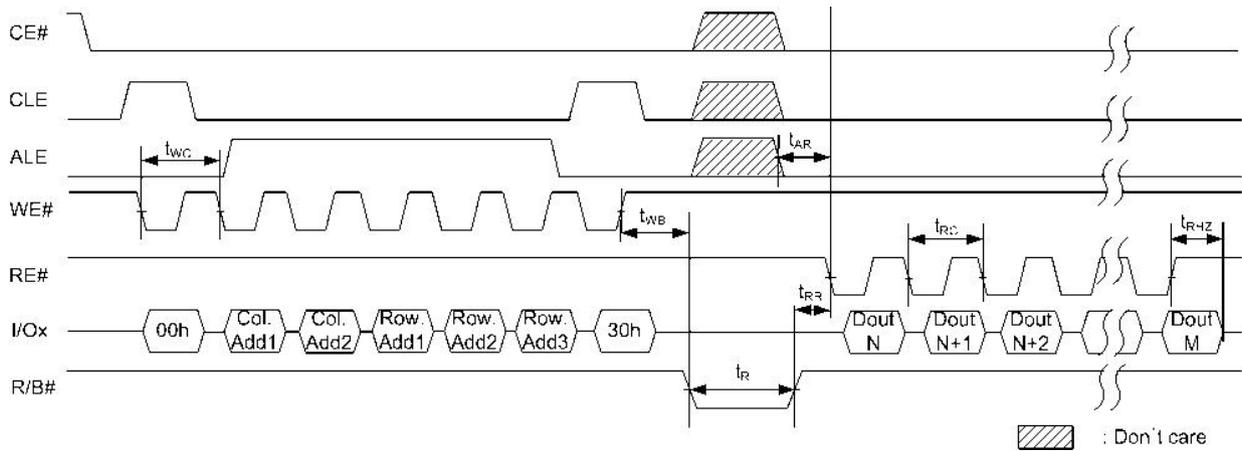
Figure 9. Page Read Operation Timings (Intercepted by CE)
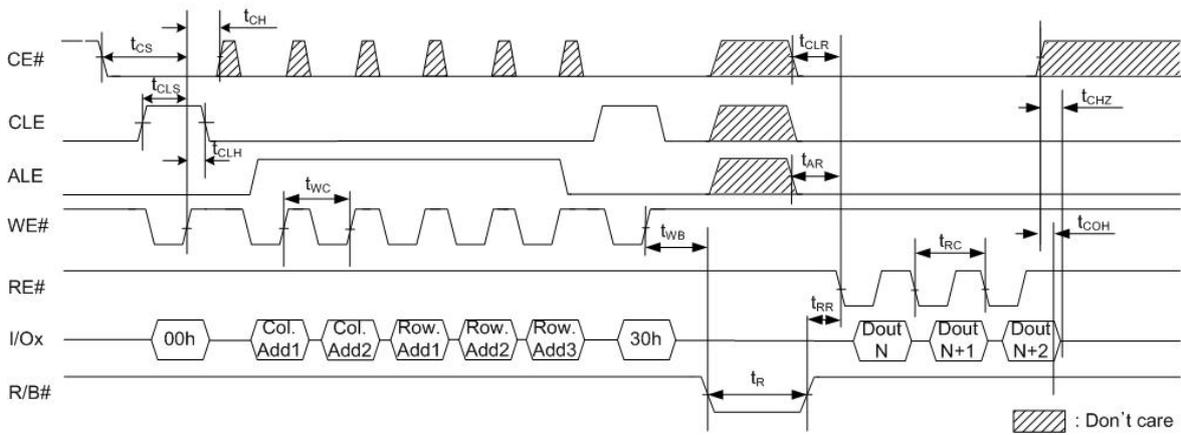
Figure 10. Page Read Operation Timings with C̅E̅ don't care
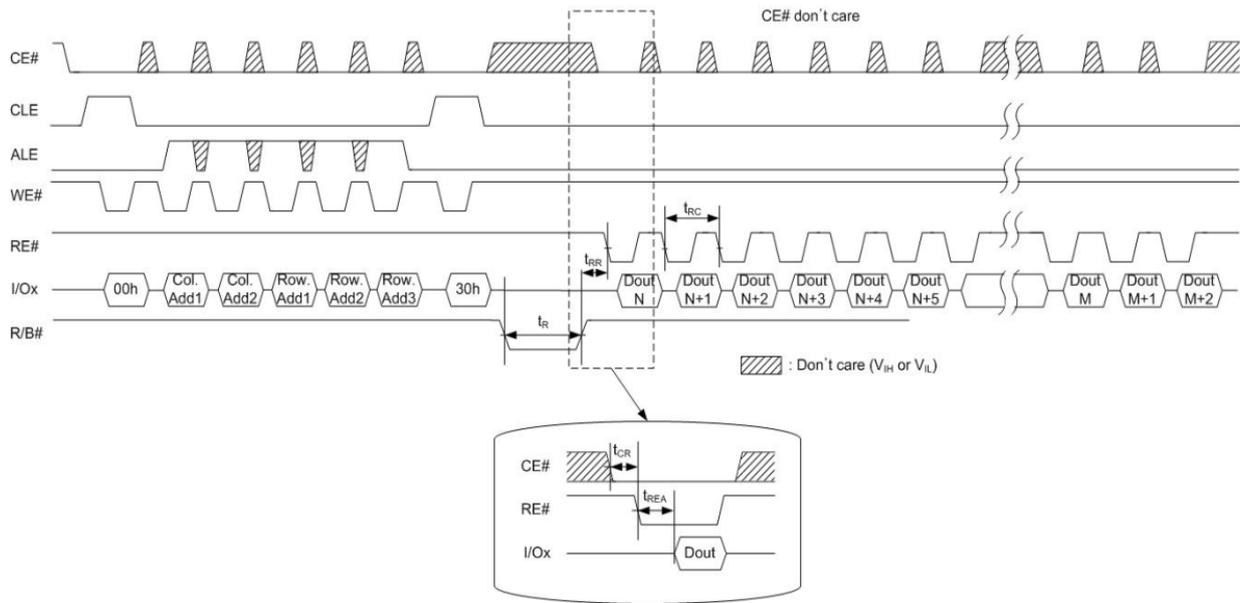
Figure 11. Random Data Output Timings
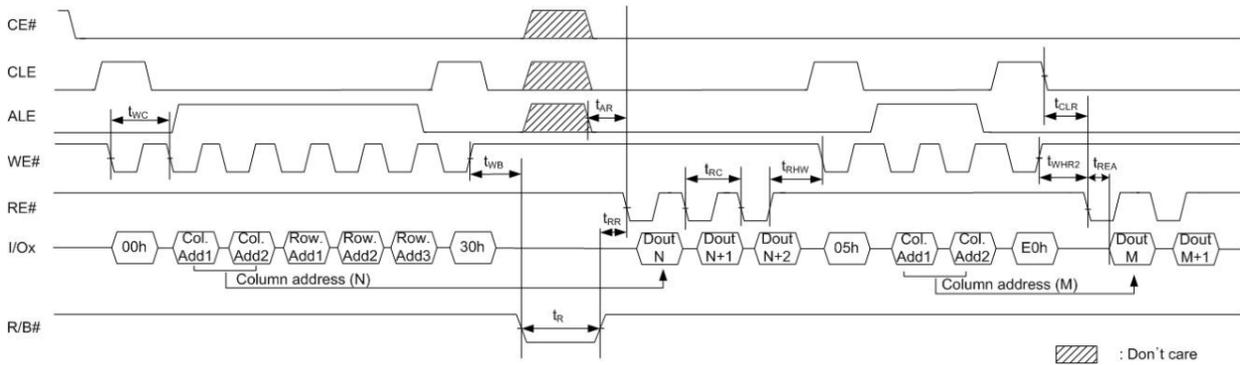
Figure 12. Multi-plane Page Read Operation with Random Data output Timings
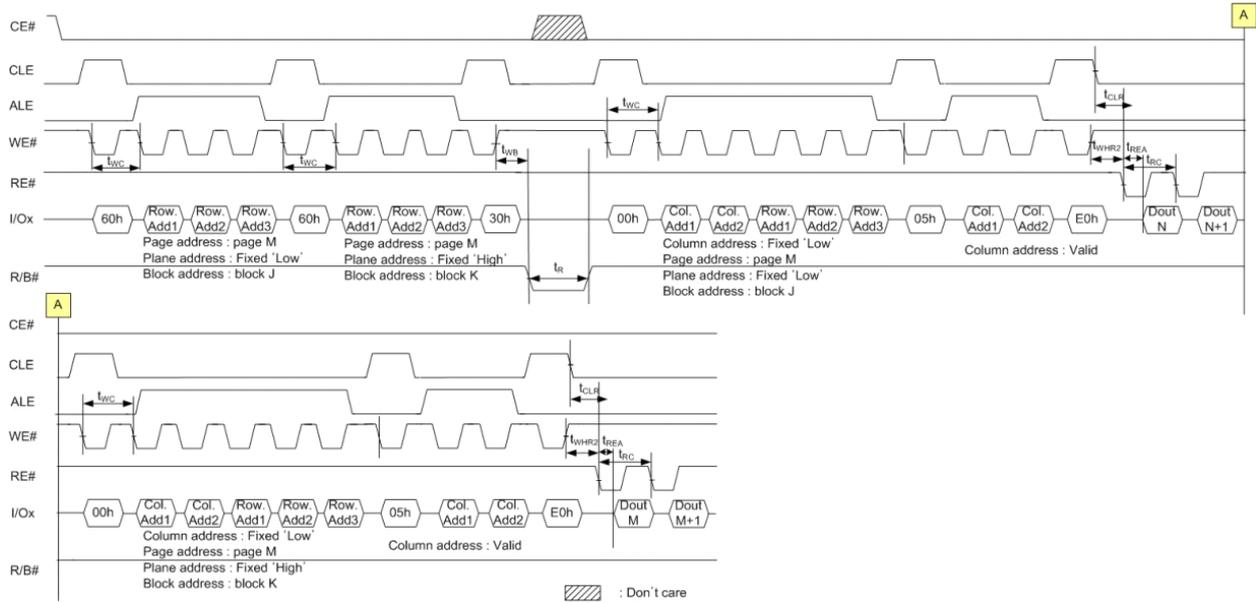
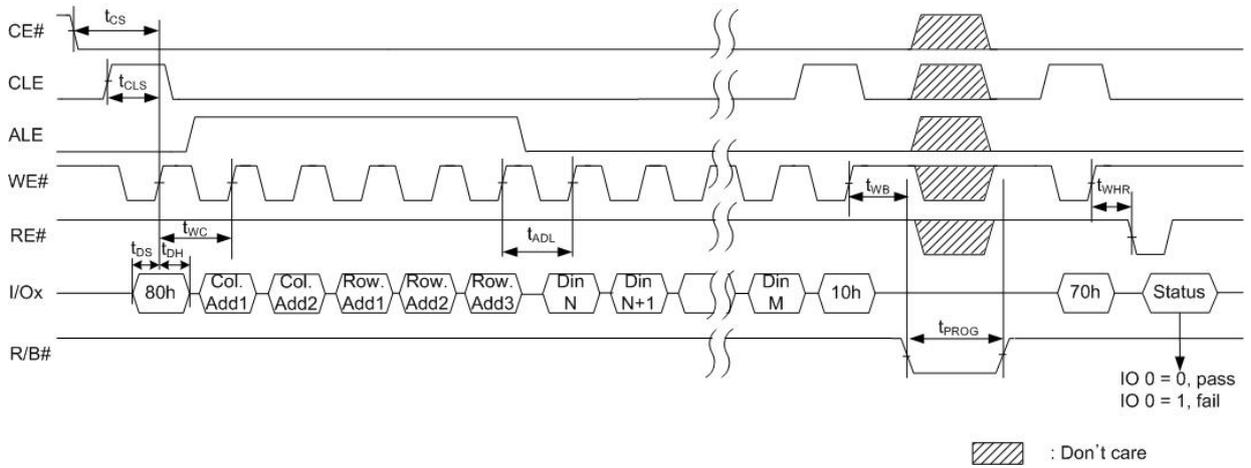## Figure 13. Cache Read Operation Timings

Figure 14. Multi Plane Cache Read Operation Timings

Figure 15. Read ID Operation Timings
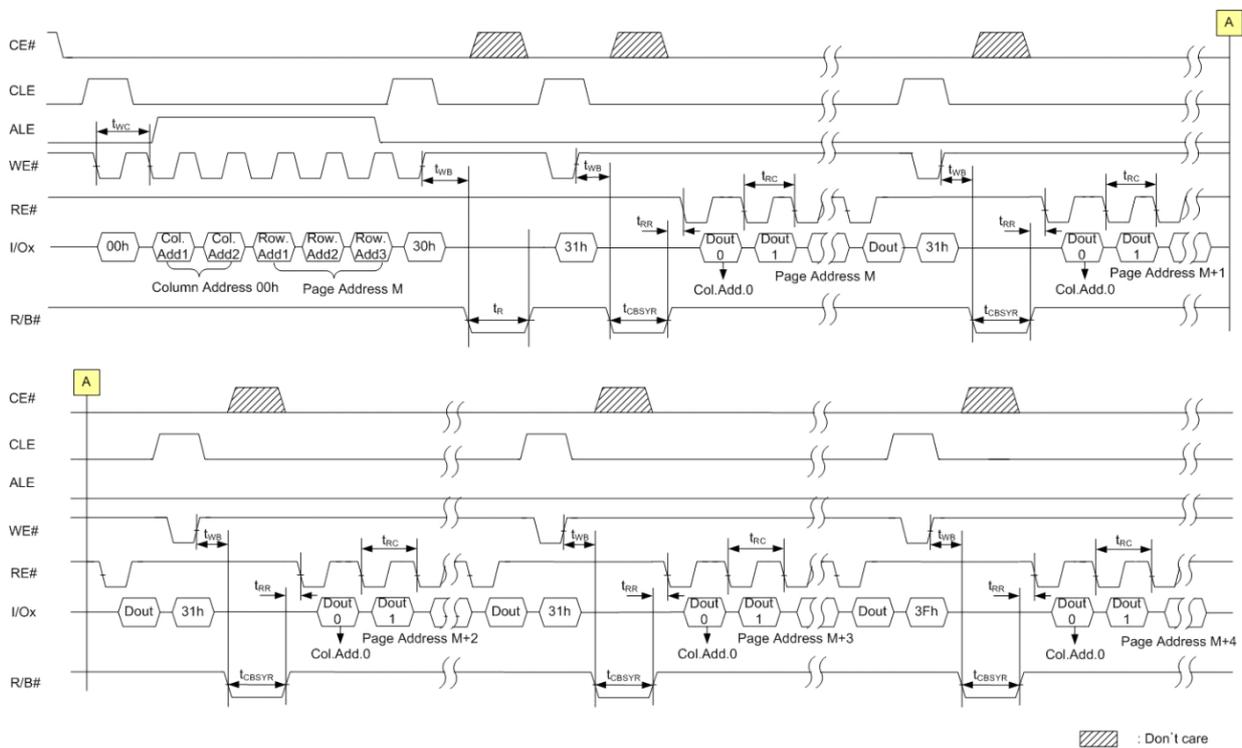
Figure 16. Page Program Operation Timings

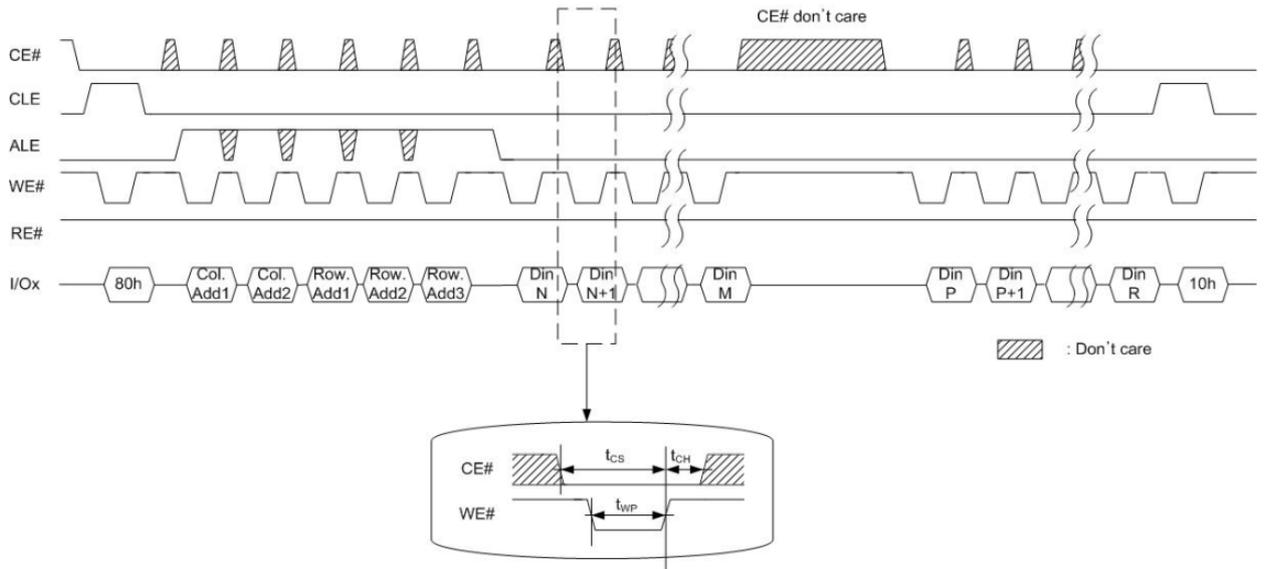**Figure 17. Page Program Operation Timings with CE don't care**
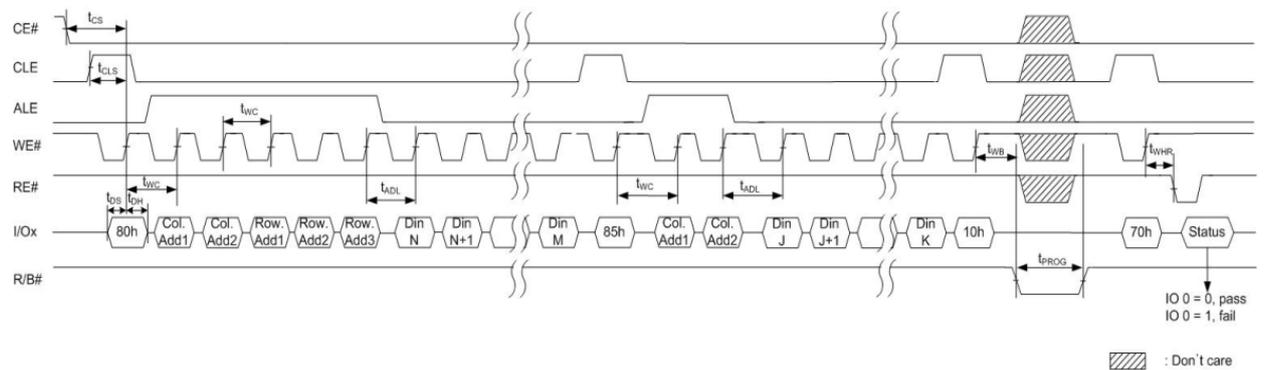

Figure 18. Random Data Input Timings

Figure 19. Multi-Plane Page Program Operation Timings

A0-A14 : Valid
A15-A22 : Valid(Page M)
A23 : Fixed 'Low'
A24 ~ A34 : Valid (Block J)

A0-A14 : Valid
A15-A22 : Valid(Page M)
A23 : Fixed 'High'
A24 ~ A34 : Valid (Block K)

IO 0 = 0, pass
IO 0 = 1, fail

Don't care

Figure 20. Copy-Back Program Operation Timings with Random Date Input

IO 0 = 0, pass
IO 0 = 1, fail

: Don't care

Figure 21. Cache Program Operation Timings
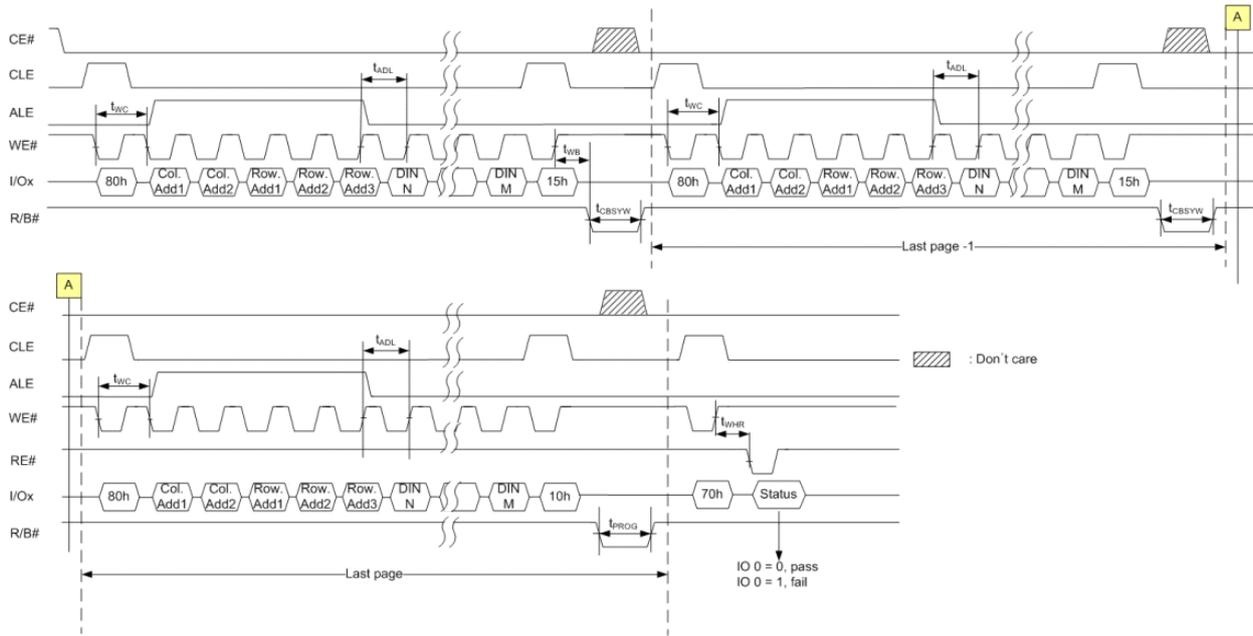
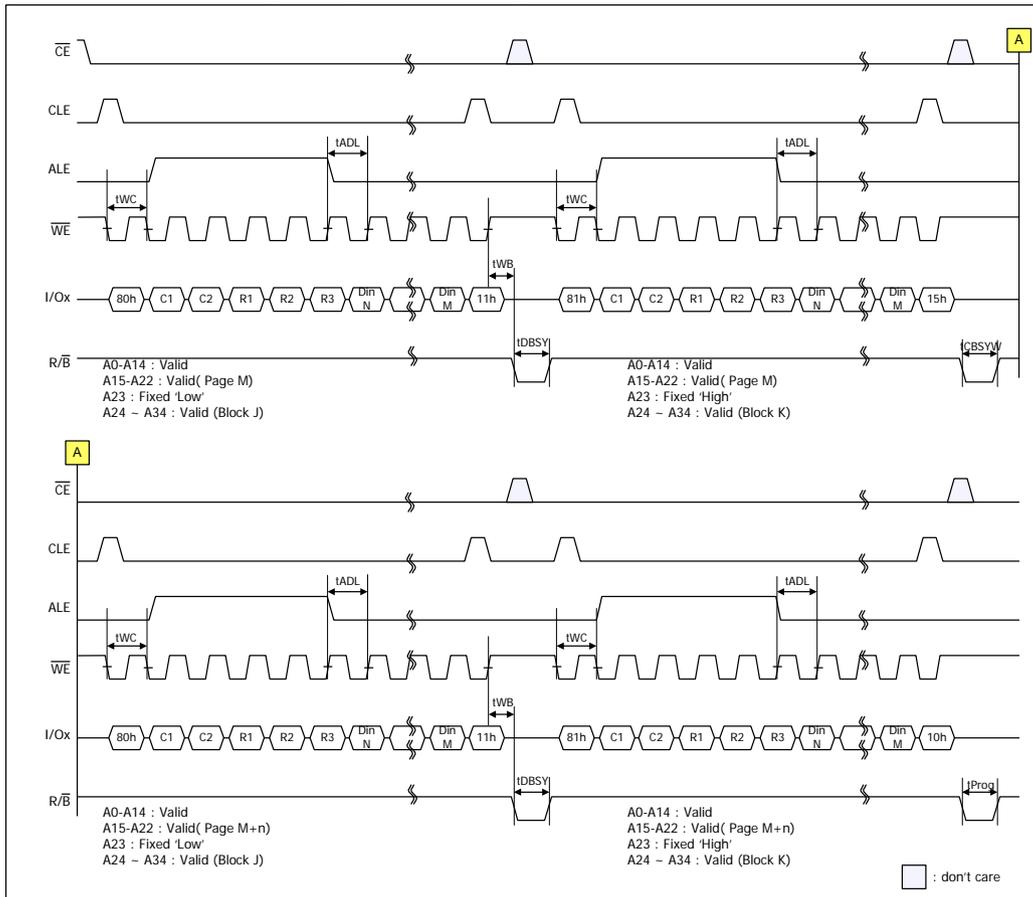## Figure 22. Multi-Plane Cache Program Operation Timings
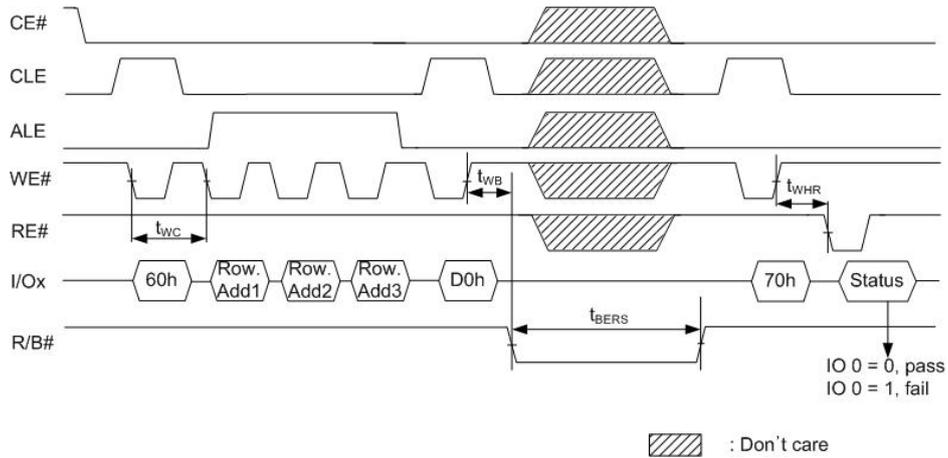
Figure 23. Block Erase Operation Timings
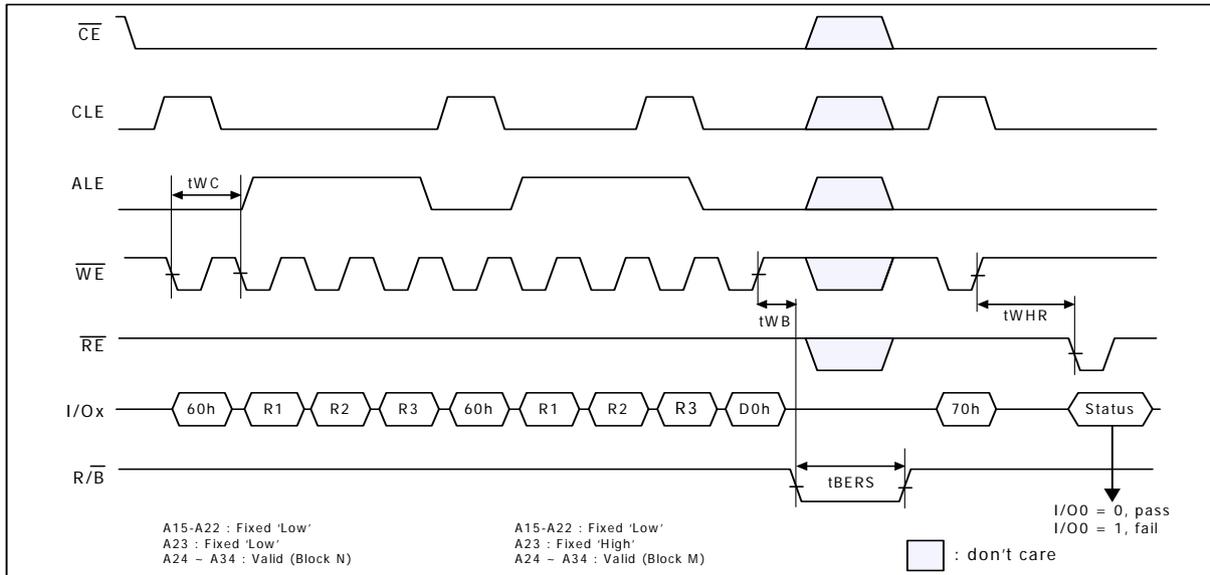

Figure 24. Multi-Plane Erase Operation Timings

Figure 25. Reset Timings