3/4-Cell Lithium-Ion/Polymer Protector

Features

- **n** High Detection Accuracy
  - -Overcharge Detection: ±25mV
  - -Overdischarge Detection: ±80mV
  - -Discharge Overcurrent Detection: ±25mV
- **n** Discharge Overcurrent Protection
- **n** High Withstand Voltage
  - -Absolute maximum ratings: 40V (VDD – VSS)
- **n** Low Supply Current
  - -Supply current: 9μA (Typ.)
  - -Standby current: 0.1μA (Max.) (Power Down Mode)
- **n** Three Types of Current Protections
- **n** Ultra Small Package
  - -TSSOP16

Descriptions

The NT1775 protects lithium-ion/lithium-polymer rechargeable battery in the abnormal events of overcharge, overdischarge, discharge overcurrent and for a 3/4-cell lithium-ion/lithium polymer battery pack.

If any of above abnormal conditions occurred. NT1775 would turn off the MOSFETs to protect battery.

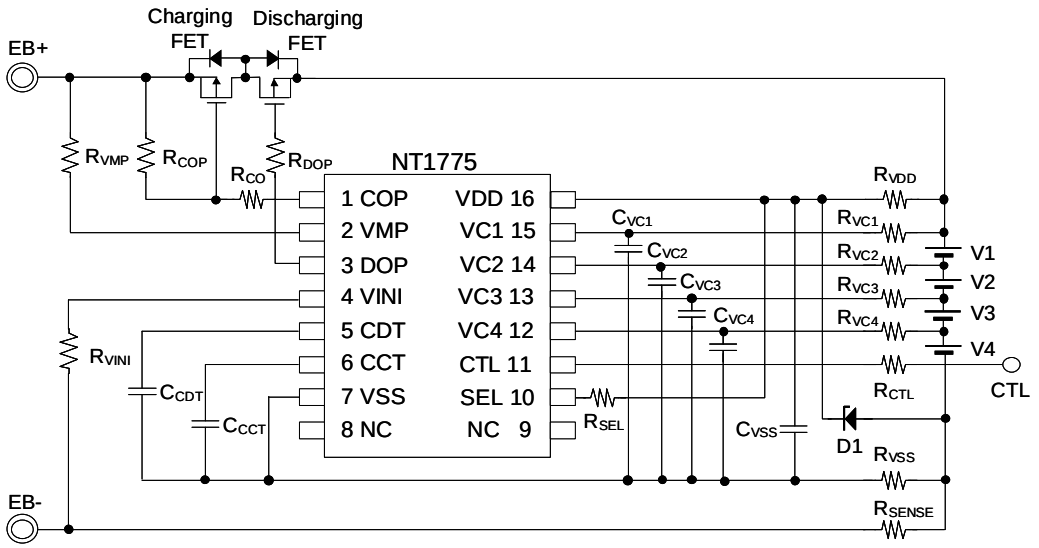
NT1775 would enter power down mode when overdischarge protection occurs to minimize the current consumption.

The tiny package of 16 pin TSSOP is especially suitable for the battery packs in portable devices.

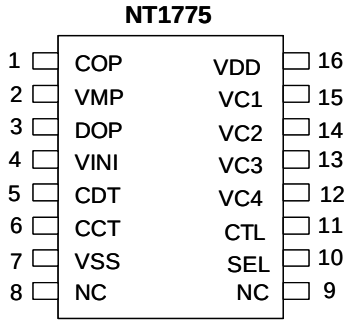
Applications

- **n** Lithium-ion rechargeable battery packs
- **n** Lithium-polymer rechargeable battery packs

Typical Application Circuit



Pins Configurations



Ordering Information

NT1775-XXX XX

Package Type
Q1: TSSOP16

Version Type

Marking Information

NT1775-XXX

Version Type

Part Number	Overcharge Detection Voltage (V_{OV})	Overcharge Release Voltage (V_{REL1})	Overdischarge Detection Voltage (V_{OD})	Overdischarge Release Voltage (V_{REL2})	Discharge Overcurrent Detection Voltage 1 (V_{DOC1})	0V Battery Charge Function
NT1775-JPM	4.275	4.075	2.3	2.7	0.130	Available
NT1775-ENK	4.350	4.150	2.4	3.0	0.150	Available
NT1775-GNG	4.300	4.150	2.4	3.0	0.200	Available

For any changes to the detection voltage or other parameters, please contact Neotec.

Pins Description

No.	Symbol	Description
1	COP	FET gate control pin for charging path (Nch open-drain output)
2	VMP	Voltage detction pin between VDD and VMP (Short-circuit detection pin)
3	DOP	FET gate control pin for discharging path (CMOS output)
4	VINI	Voltage detction pin between VSS and VINI (Overcurrent 1,2 detection pin)
5	CDT	Capacitor connection for overdischarge detection, overcurrent detection 1 delay time
6	CCT	Capacitor connection for overcharge detection delay time
7	VSS	Negative power input pin
8	NC	No connection
9	NC	No connection
10	SEL	Pin for switching 3cell/4cell series SEL pin=VSS: 3cell, SEL pin=VDD: 4cell
11	CTL	Control of charge FET and discharge FET CTL Pin / COP Pin / DOP Pin High / Hi-Z / VDD Open / Hi-Z / VDD Low / Normal status* / Normal status*
12	VC4	Cell 4 positive voltage and cell 3 negative voltage input pin
13	VC3	Cell 3 positive voltage and cell 2 negative voltage input pin
14	VC2	Cell 2 positive voltage and cell 1 negative voltage input pin
15	VC1	Cell 1 positive voltage input pin
16	VDD	Power supply input pin

Absolute Maximum Ratings

Symbol	Descriptions		Rating	Units
VDD	Input voltage between VDD and VSS		Vss – 0.3 to Vss + 40	V
V_{IN}	Input Voltage	VC1, VC2, VC3, VC4, CTL, SEL	Vss - 0.3 to VDD + 0.3	V
		CCT, CDT, VINI pins	Vss - 0.3V to Vss + 8.0V	
V_{VMP}		VMP pin	Vss – 0.3 to Vss + 40	V
V_{CO}	Output Voltage	COP pin	Vss –0.3 to Vss + 40	V
V_{DO}		DOP pin	Vss - 0.3 to VDD + 0.3	V
P_D	Power Dissipation		400	mW
T_{OPT}	Operating Temperature Range		-40 to +85	°C
T_{STG}	Storage Temperature Range		-55 to +125	°C

Applying any over “Absolute Maximum Ratings” practices can possibility damage the device. These data are indicated the absolute maximum values only but not implied any operational performance.

Electrical Characteristics

(Ta = 25°C)

Symbol	Item	Conditions	MIN	TYP	MAX	Unit
Detection Voltage						
V_{OV}	Overcharge detection voltage	-	V_{OV} – 0.025	V_{OV}	V_{OV} + 0.025	V
V_{REL1}	Overcharge release voltage	-	V_{REL1} – 0.050	V_{REL1}	V_{REL1} + 0.050	V
V_{OD}	Overdischarge detection voltage	-	V_{OD} – 0.080	V_{OD}	V_{OD} + 0.080	V
V_{REL2}	Overdischarge release voltage	-	V_{REL2} – 0.100	V_{REL2}	V_{REL2} + 0.100	V
V_{DOC1}	Discharge overcurrent detection voltage 1	-	V_{DOC1} – 0.025	V_{DOC1}	V_{DOC1} + 0.025	V
V_{DOC2}	Discharge overcurrent detection voltage 2	-	0.4	0.5	0.6	V
V_{SHORT}	Short detection voltage	VDD reference	0.9	1.2	1.5	V
Delay Time						
t_{OV}	Output delay time of overcharge	CCT pin capacitance=0.1μF	0.5	1.0	1.5	s
t_{OD}	Output delay time of overdischarge	CDT pin capacitance=0.1μF	50	100	150	ms
t_{DOC1}	Output delay time of discharge over current 1		5	10	15	ms
t_{DOC2}	Output delay time of discharge over current 2	-	0.4	1	1.6	ms
t_{SHORT}	Output delay time of short detection	FET gate capacitance=2000pF	100	300	600	μs
Current Consumption						
I_{DD}	Supply current	V1=V2=V3=V4=3.5V	-	9	15	μA
I_{PDN}	Current consumption at power down	V1=V2=V3=V4=1.5V	-	-	0.1	μA
I_{VC1}	VC1 pin current	V1=V2=V3=V4=3.5V	-0.3	0	0.3	μA
I_{VC2}	VC2 pin current	V1=V2=V3=V4=3.5V	-0.3	0	0.3	μA
I_{VC3}	VC3 pin current	V1=V2=V3=V4=3.5V	-0.3	0	0.3	μA
I_{VC4}	VC4 pin current	V1=V2=V3=V4=3.5V	-0.3	0	0.3	μA
I_{CTLH}	CTL pin current "H"	V1=V2=V3=V4=3.5V V_{CTL}=VDD	-	-	0.1	μA
I_{CTLL}	CTL pin current "L"	V1=V2=V3=V4=3.5V $V_{CTL}=V_{SS}$	-0.8	-	-	μA
I_{SELH}	SEL pin current "H"	V1=V2=V3=V4=3.5V V_{SEL}=VDD	-	-	0.1	μA
I_{SELL}	SEL pin current "L"	V1=V2=V3=V4=3.5V $V_{SEL}=V_{SS}$	-0.1	-	-	μA
Input Voltage						
VDD	Operating voltage between VDD and VSS	Output voltage of COP and DOP fixed	4.0	-	26	V
V_{CTLH}	CTL input voltage "H"	-	2.7	-		V
V_{CTLL}	CTL input voltage "L"	-		-	1	V
V_{SELH}	SEL input voltage "H"	-	VDD × 0.8	-		V
V_{SELL}	SEL input voltage "L"	-		-	VDD × 0.2	V

Electrical Characteristics (continued)

Symbol	Item	Conditions	MIN.	TYP.	MAX.	Unit
0V Battery Charging Function						
V_{0CHA}	0V battery charge starting charger voltage	0V battery charging available	-	1.6	2.0	V
V_{0INH}	0V battery charge inhibition battery voltage	0V battery charging unavailable	-	-	1.4	V
Output Current						
I_{COH}	COP pin leakage current	V_{COP}=24V	-	-	0.1	μA
I_{COL}	COP pin sink current	V_{COP}=V_{SS}+0.5V	10	-	-	μA
I_{DOH}	DOP pin source current	V_{DOP}=VDD-0.5V	10	-	-	μA
I_{DOL}	DOP pin sink current	V_{COP}=V_{SS}+0.5V	10	-	-	μA
VMP Internal Resistance						
R_{VMD}	Internal resistance between VMP and VDD	V1=V2=V3=V4=3.5V	0.5	1	1.5	MΩ
R_{VMS}	Internal resistance between VMP and V_{SS}	V1=V2=V3=V4=1.8V	450	900	1800	KΩ

(1) Short-circuit detection delay time is time between VMP and DOP changes

Measurement Methods

(1) Measurement 1 (Measurement circuit 1)

1) Set V1=V2=V3=V4=3.5V, S1=ON and S2=OFF, enter normal condition.
2) The measured current at VSS pin is the supply current (I_{DD})
3) Set V1=V2=V3=V4=1.5V, S1=OFF and S2=ON, enter power down mode.
4) The measured current at VSS pin is the current consumption at power down (I_{PDN})

(2) Measurement 2 (Measurement circuit 2)

1) Set V1=V2=V3=V4=3.5V, V_{SEL}=VDD, V_{VMP}=V_{VINI}=V_{CTL}=0V and S1=OFF, enter normal condition.
2) Initialize V1 voltage from 3.5V and increase gradually. The V1 voltage is the overcharge detection voltage (V_{OV}) when COP pin switches from low to high.
3) Decrease V1 gradually. The V1 voltage is the overcharge release detection voltage (V_{REL1}) when COP pin switches from high to low.
4) Further decrease V1. The V1 voltage is the overdischarge detection voltage (V_{OD}) when DOP pin switches from low to high. Increase V1 gradually. When DOP pin switches from high to low, the V1 voltage is the overdischarge release detection voltage (V_{REL2}).
   When the voltage of Vn (n=2 to 4) is changed. The overcharge detection/release voltage (V_{OV}/V_{REL1}) overdischarge detection/release voltage (V_{OD}/V_{REL1}) can be determined in the same way as when n=1.

(3) Measurement 3 (Measurement circuit 2)

1) Set V1=V2=V3=V4=3.5V, V_{SEL}=VDD, V_{VMP}=V_{VINI}=V_{CTL}=0V, S1=OFF, enter normal condition.
2) Initialize V_{VINI} from 0V and increase gradually. When both COP and DOP pins switch from low to high, the V_{VINI} voltage is the discharge overcurrent detection voltage1 (V_{DOC1}).

(4) Measurement 4 (Measurement circuit 2)

1) Set V1=V2=V3=V4=3.5V, V_{SEL}=VDD, V_{VMP}=V_{VINI}=V_{CTL}=0V, S1=ON, enter normal condition.
2) Initialize V_{VINI} from 0V and increase gradually. When both COP and DOP pins switch from low to high, the V_{VINI} voltage is the discharge overcurrent detection voltage2 (V_{DOC2}).

(5) Measurement 5 (Measurement circuit 2)

1) Set V1=V2=V3=V4=3.5V, V_{SEL}=VDD, V_{VMP}=V_{VINI}=V_{CTL}=0V, S1=OFF, enter normal condition.
2) Initialize V_{VMP} from 0V and increase gradually. When both COP and DOP pins switch from low to high, the V_{VMP} voltage is the short detection voltage (V_{SHORT}).

(6) Measurement 6 (Measurement circuit 2)

1) Set V1=V2=V3=V4=3.5V, V_{SEL}=VDD, V_{VM}=V_{VINI}=V_{CTL}=0V, S1=OFF, enter normal condition.
2) Initialize V_{CTL} from 0V and increase gradually. When both COP and DOP pins switch from low to high, the V_{CTL} voltage is the CTL input voltage “H” (V_{CTLH}).
3) Decrease V_{CTL} from VDD gradually. When both COP and DOP pins switch from high to Low, the V_{CTL} is the CTL input voltage “L” (V_{CTLL}).

(7) Measurement 7 (Measurement circuit 2)

1) Set V1=V2=V3=3.5V, V4=V_{SEL}=0V, V_{VMP}=V_{VINI}=V_{CTL}=0V, S1=OFF, enter normal condition.
2) Decrease V_{SEL} from VDD gradually. When DOP pin switches from high to Low, the V_{SEL} is the SEL input voltage “L” (V_{SELL}).
3) Initialize V_{SEL} from 0V and increase gradually. When DOP pin switches from low to high, the V_{SEL} voltage is the SEL input voltage “H” (V_{SELH}).

(8) Measurement 8 (Measurement circuit 3)

1) Set V1=V2=V3=V4=3.5V, V_{VMP}=V_{VINI}=0V, S1=ON. S2=OFF, enter normal condition.
2) Increase V1 from 3.5V to 4.4V immediately (within 10us). The overcharge detection delay time (t_{OV}) is the period from the time V1 gets to 4.4V till COP pin switches from high to low.
3) Set V1=3.5V, V2=0V, S1=ON and S2 = OFF, enter normal condition.
4) Decrease V1 from 3.5V to (V_{OD}-0.1V) immediately (within 10us). The overdischarge detection delay time (t_{OD}) is the period from the time V1 gets to (V_{OD}-0.1V) till DOP pin switches from high to low.

(9) Measurement 9 (Measurement circuit 3)

1) Set V1=V2=V3=V4=3.5V, V_{VMP}=V_{VINI}=0V, S1=ON. S2=OFF, enter normal condition.
2) Increase V_{VINI} from 0V to V_{DOC1} (Max.)+10mV immediately (within 10us). The discharge overcurrent detection delay time 1 (t_{DOC1}) is the period from the time V_{VINI} gets to V_{DOC1} (Max.)+10mV till COP and DOP pin switches from low to high.
3) Set V1=V2=V3=V4=3.5V, V_{VMP}=V_{VINI}=0V, S1=OFF. S2=ON, enter normal condition.
4) Increase V_{VINI} from 0V to V_{DOC2} (Max.)+0.1V immediately (within 10us). The discharge overcurrent detection delay time 2 (t_{DOC2}) is the period from the time V_{VINI} gets to V_{DOC2} (Max.)+0.1V till COP and DOP pin switches from low to high.
5) Set V1=V2=V3=V4=3.5V, V_{VMP}=V_{VINI}=0V, S1=OFF. S2=ON, enter normal condition.
6) Increase V_{VMP} from 0V to 1.7V immediately (within 10us). The short detection delay time (t_{SHORT}) is the period from the time V_{VMP} gets to 1.7V till COP and DOP pin switches from low to high.

(10) Measurement 10 (Measurement circuit 4)

1) Set V1=V2=V3=V4=3.5V, V_{COP}=V_{DOP}=V_{VMP}=V_{CTL}=0V, V_{SEL}=VDD. VDD/I_{VMD} is the internal resistance between VDD and VMP (R_{VMD}).
2) Set V1=V2=V3=V4=1.8V, V_{COP}= V_{CTL}=0V, V_{DOP}=V_{VMP}=V_{SEL}=VDD. VDD/I_{VMS} is the internal resistance between VSS and VMP (R_{VMS}).

(11) Measurement 11 (Measurement circuit 4)

1) Set V1=V2=V3=V4=3.5V, V_{COP}=V_{DOP}=V_{CTL}=0V, V_{SEL}=V_{VMP}=VDD, the current flowing through the CTL pin is the CTL pin current "L" (I_{CTLL}). Then, set V_{CTL}=VDD, the current flowing through the CTL pin is the CTL pin current "H" (I_{CTLH}).
2) Set V1=V2=V3=V4=3.5V, V_{COP}=V_{DOP}=V_{CTL}=0V, V_{SEL}=V_{VMP}=VDD, the current flowing through the SEL pin is the SEL pin current "H" (I_{SELH}). Then, set V_{SEL}=0V, the current flowing through the SEL pin is the SEL pin current "L" (I_{SELL}).

(12) Measurement 12 (Measurement circuit 4)

1) Set V1=V2=V3=V4=6V, V_{DOP}=V_{CTL}=0V, V_{SEL}=V_{VMP}=V_{COP}=VDD, the current flowing through the COP pin is the COP pin leakage current (I_{COH}). Then, set V_{COP}=Vss+0.5V, the current flowing through the COP pin is the COP pin sink current (I_{COL}).
2) Set V1=V2=V3=V4=3.5V, V_{CTL}=0V, V_{SEL}=V_{COP}=VDD, V_{VMP}=VDD-2V, V_{DOP}=VDD-0.5V, the current flowing through the DOP pin is the DOP pin source current (I_{DOH}). Then, set V_{VMP}=VDD, V_{DOP}=Vss+0.5V, the current flowing through the DOP pin is the DOP pin sink current (I_{DOL}).

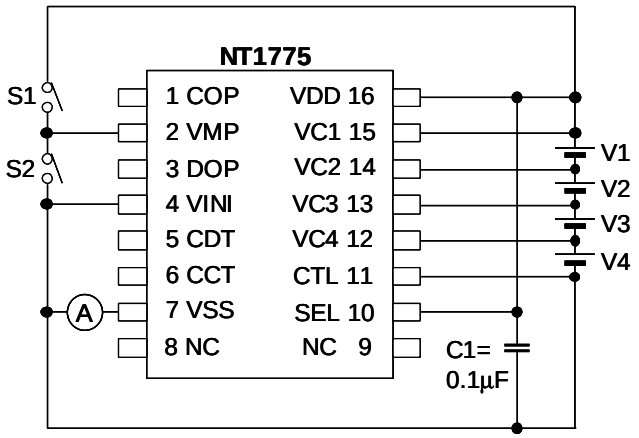
(13) Measurement 13 (Measurement circuit 5)

1) Set V1=V2=V3=V4=0V, increase V_{VMP} from 0V gradually.
2) The V_{VMP} voltage is the 0V charge starting voltage (V_{0CHA}) when COP pin voltage is 1V lower than the V_{VMP} voltage.

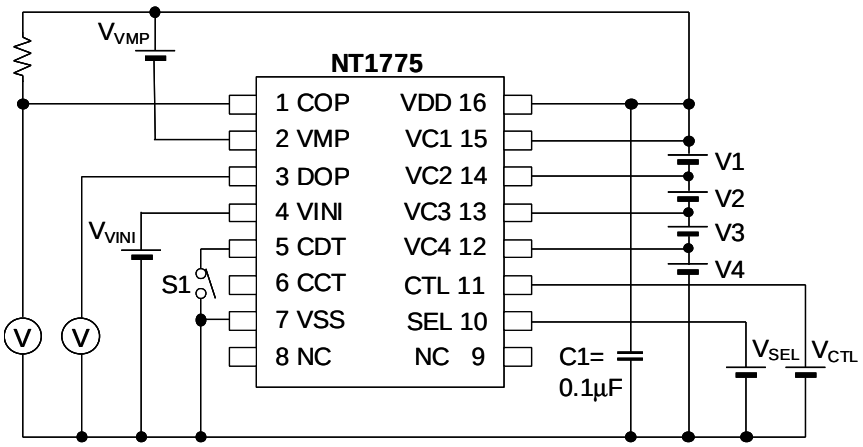
(14) Measurement 14 (Measurement circuit 5)

1) Set V1=V2=V3=V4=24V, increase V_{VMP} from 0V gradually.
2) The V1 voltage is the 0V charge inhibition voltage (V_{0INH}) when COP pin voltage should be higher than V_{VMP}-1V.

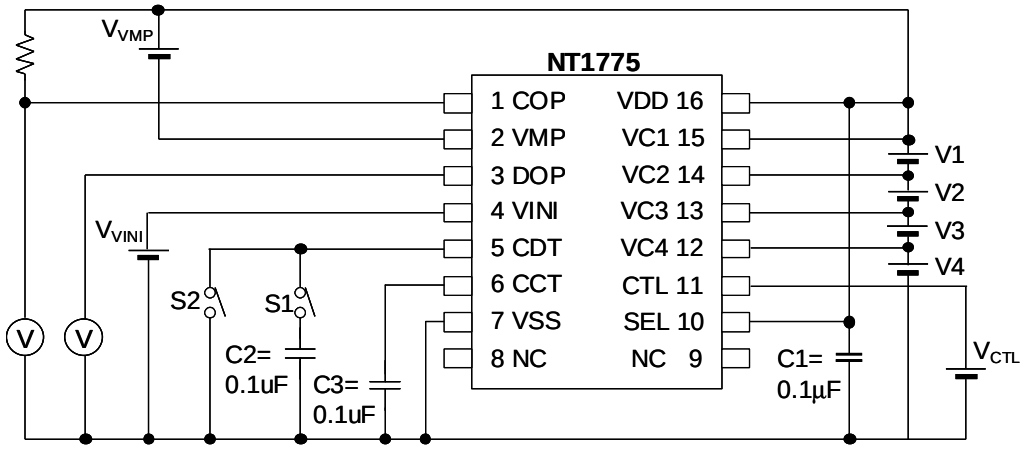
Measurement Circuit



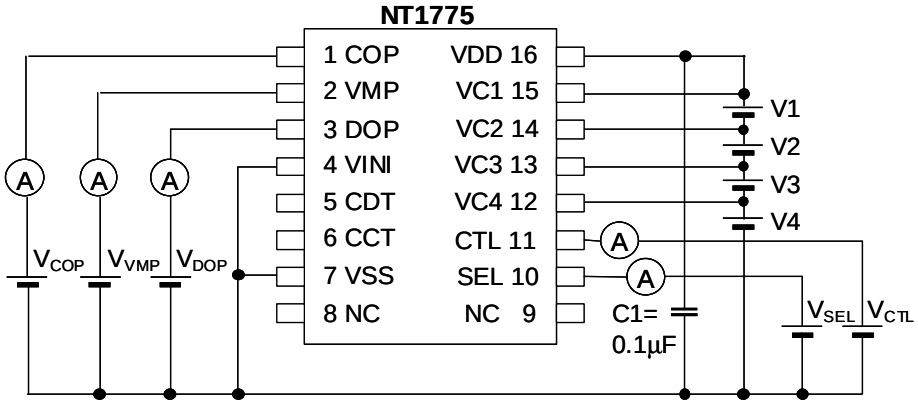
Measurement circuit 1



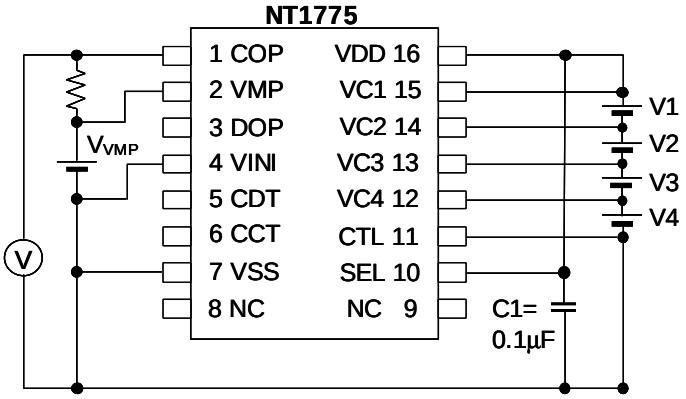
Measurement circuit 2



Measurement circuit 3

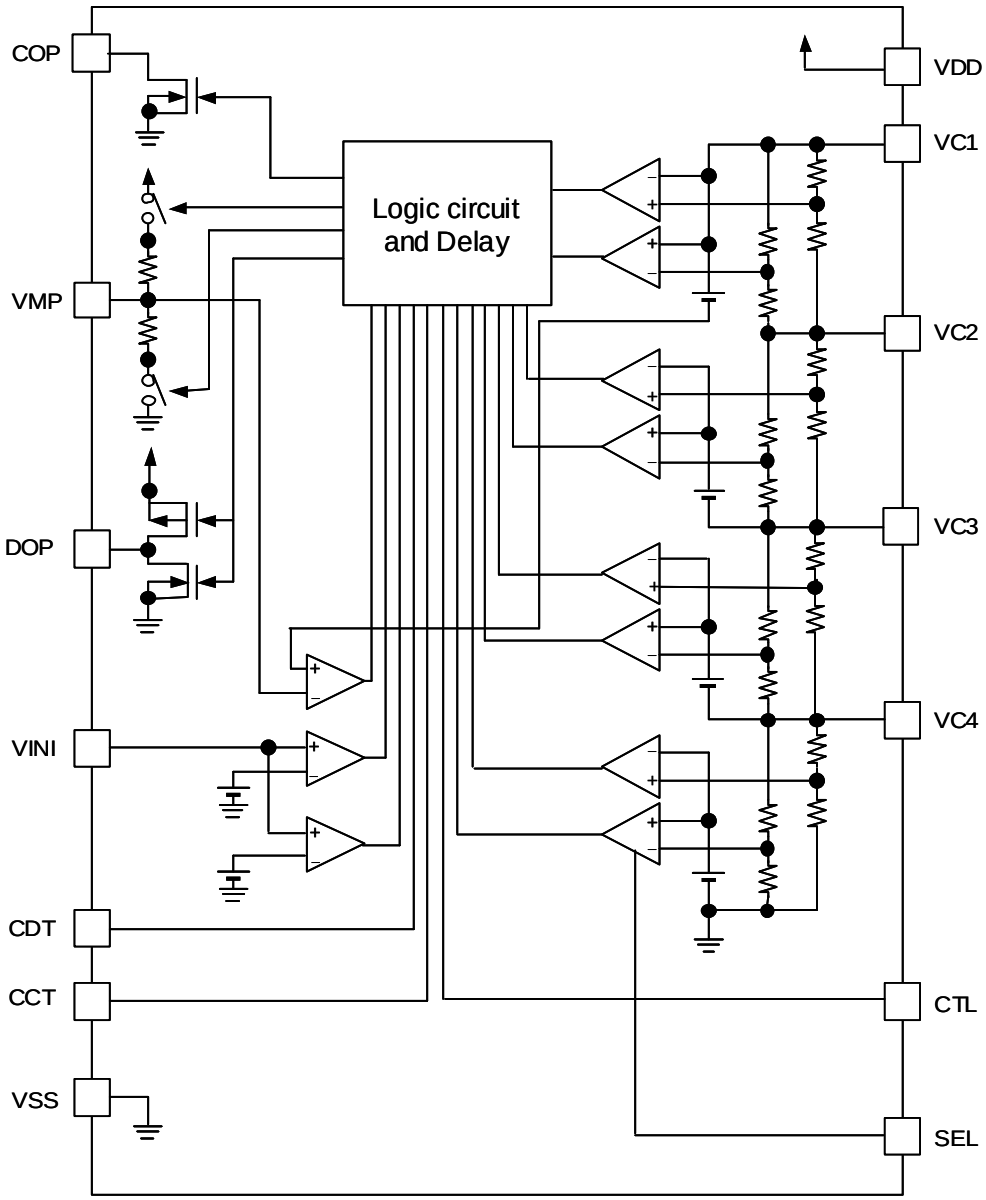


Measurement circuit 4



Measurement circuit 5

Block Diagram



Operations

The NT1775 provides overcharge, overdischarge, discharge overcurrent, and short circuit protections for the 3/4-cell battery pack. When the battery pack is in charging stage, the current flow is from EB+ to EB- through the batteries. NT1775 continuously senses all the battery voltage by VC1~VC4 pins if the overcharge occurs. On the other hand, when the battery pack is in discharging stage, the current flow is from EB+ to EB- through the load. NT1775 also senses all battery voltages by VC1~VC4 pins if the overdischarge occurs. As discharging, there is a positive voltage between VSS and EB-, because the current passing through R_{SENSE}. NT1775 detects this positive voltage by VINI pin if the discharge overcurrent occurs as well. Further, NT1775 also provide a short protection by detecting the voltage drop between VDD and VMP pins.

(1) Overcharge Condition

1) Overcharge Protection

When any of the cells voltage is equal to or higher than the overcharge detection voltage (V_{OV}) for a certain delay time (t_{OV}), NT1775 would turn off the external Pch MOSFET by COP pin to protect the pack from being overcharged. In the meanwhile, COP pin turns to “H” from “L” level.

2) Overcharge Protection Release

The overcharge protection can be released by either of the following conditions,

(a) Removed charger and connect a load (100KΩ typically) when all battery voltages are lower than the detection voltage V_{OV}

(b) All battery voltages are lower than the overcharge release voltages V_{REL1}.

(2) Overdischarge Condition

1) Overdischarge Protection

When any of the cells is lower than the overdischarge detection voltage (V_{OD}) for a certain delay time (t_{OD}), NT1775 would turn off the external Pch MOSFET by DOP pin to protect the pack from being overdischarged.

2) Overdischarge Protection Release

The overdischarge protection can be released by connecting a charger when all battery voltages are equal to or higher than the overdischarge detection voltage (V_{OD}).

(3) Power Down Condition

1) Entering to Power Down Mode

NT1775 enters to the power down mode when overdischarge protection occurs. The VMP pin voltage would be pulled low through the R_{VMS} resister and the internal circuits would be turned off; therefore, the standby current consumption of NT1775 could be reduced to lower than 100nA (Max.).

2) Power Down Mode Release

The power down mode would be released when a charger is connected with the condition that the VMP pin voltage is around VDD/2 or higher.

(4) Discharge Overcurrent Condition

1) Discharge Overcurrent Protection

The NT1775 provides 3 levels of discharge overcurrent protection - discharge overcurrent 1, discharge overcurrent 2 and short circuit protection. When any of the discharge overcurrent conditions happens, the level of DOP pin would become to "H" from "L" to turn off the MOSFET to cut off the discharge path.

a) Discharge overcurrent 1 protection happens when VINI pin voltage is in the condition of $V_{DOC1} \leqq V_{VINI} < V_{DOC2}$ and lasts for a delay time longer than the specified delay time (t_{DOC1}).

b) Discharge overcurrent 2 protection starts when VINI pin voltage is in the condition of $V_{DOC2} \leqq V_{VINI} < V_{SHORT}$ and for lasts for a delay time longer than the specified delay time (t_{DOC2}).

c) Short circuit protection occurs when VMP pin voltage is in the condition of $VDD-V_{VMP} \geqq V_{SHORT}$ and for lasts for a delay time longer than the specified delay time (t_{SHORT}).

2) Discharge Overcurrent Protection Release

Any of the discharge overcurrent/short protections would be released to the normal mode when the load current reduces to the specified current (load resistance > 30MΩ) or the voltage drop between VDD and V_{VMP} pins is lower than V_{SHORT}.

(5) 0 V Battery Charge Function

NT1775 provides a 0 V battery charge function which the batteries can be charged when the charger voltage is higher than V_{0CHA}.

(6) Delay Time Setting

The overcharge delay time (t_{OV}) depend on the external capacitor's capacitance value to the CCT pin. The overdischarge detection delay time (t_{OD}) and the discharge overcurrent delay time 1 (t_{DOC1}) depend on the external capacitor's capacitance value to the CDT pin. The other delay times, discharge overcurrent delay time 2 (t_{DOC2}), and short detection delay time (t_{SHORT}) are internally fixed.

	Min.	Typ.	Max.	
t_{OV} [s] =	(5.00,	10.0,	15.0)	x CCCT [μF]
t_{OD} [s] =	(0.50,	1.00,	1.50)	x CCDT [μF]
t_{DOC1} [s] =	(0.05,	0.10,	0.15)	x CCDT [μF]

Note: The capacitance deviation of the capacitors is not included in the equation above.

(7) CTL pin

NT1775 provides a CTL pin to control the DOP and COP status. This control function takes precedence over all of the protection functions.

Conditions set by CTL pin

CTL Pin	COP Pin	DOP Pin
High	Hi-Z	VDD
Open	Hi-Z	VDD
Low	Normal status*	Normal status*

* The all detection circuits take control of the normal status.

(8) SEL pin

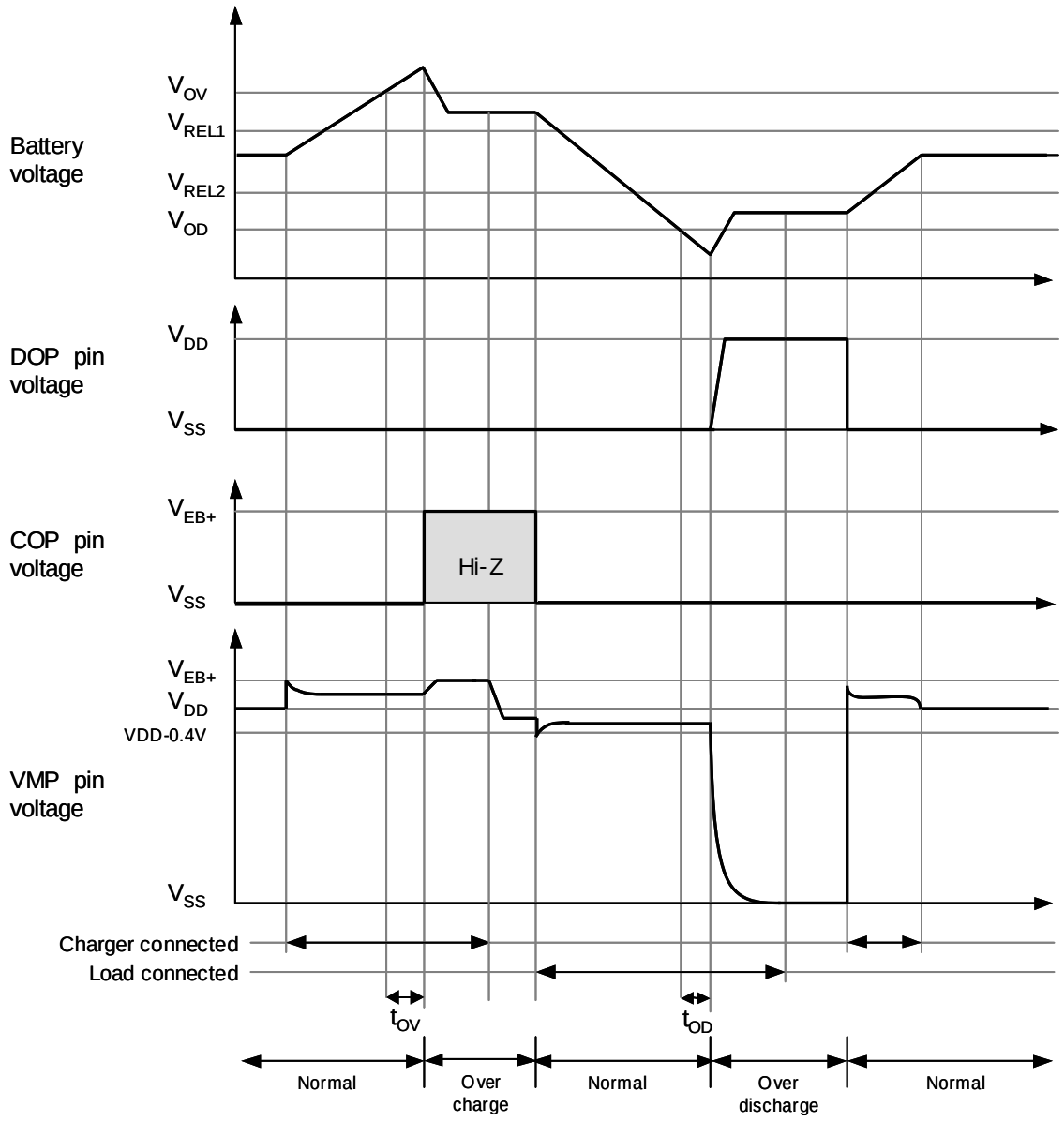
SEL pin is used to switch 4-cell application to the 3-cell. VC4 pin's detection function is prohibited when the SEL pin is connected to the VSS.

Conditions Set by SEL pin

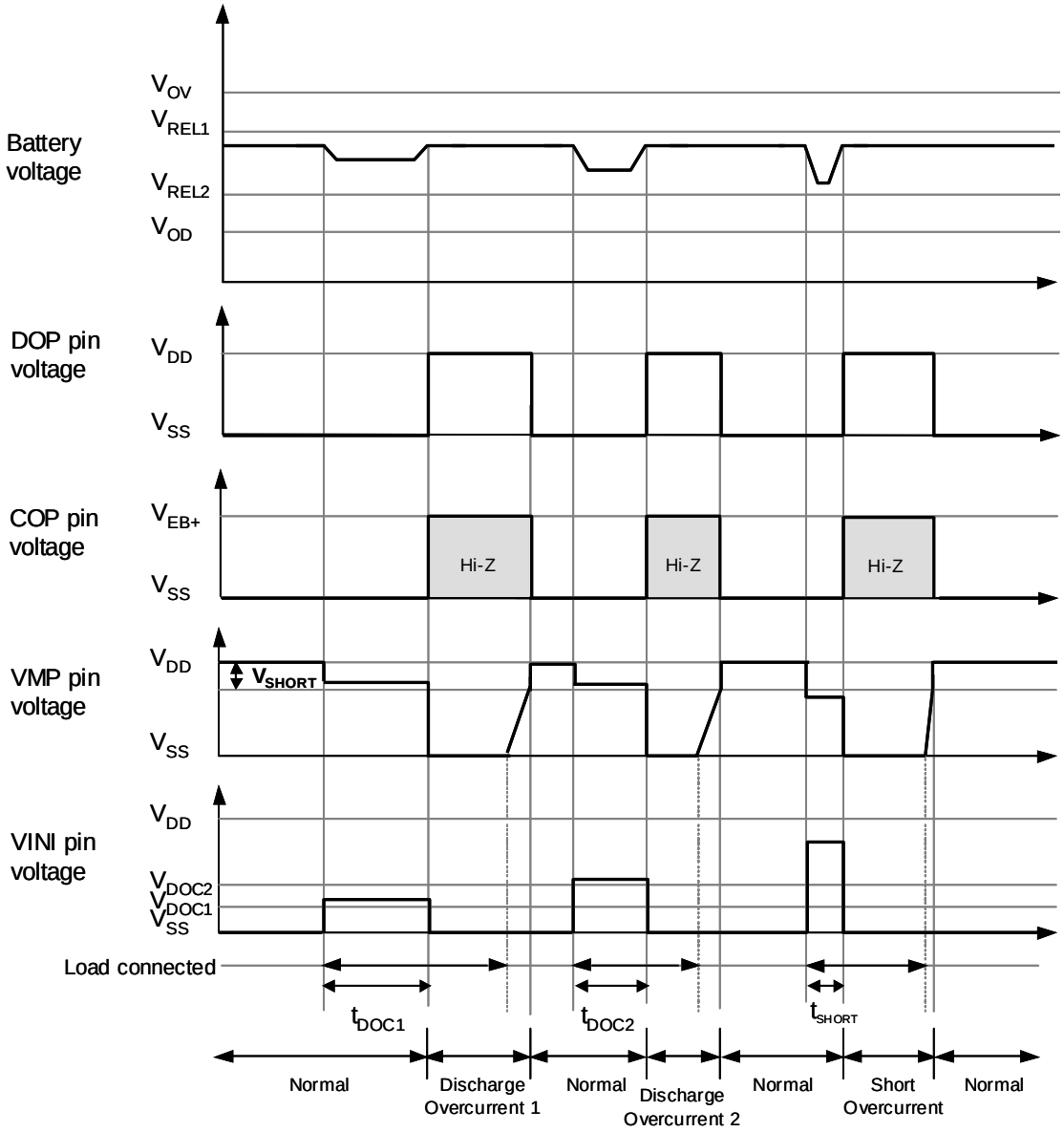
SEL Pin	Condition
High	4-cell protection
Open	Undefined
Low	3-cell protection

Operation Timing Charts

(1) Overcharge Detection, Overdischarge Detection

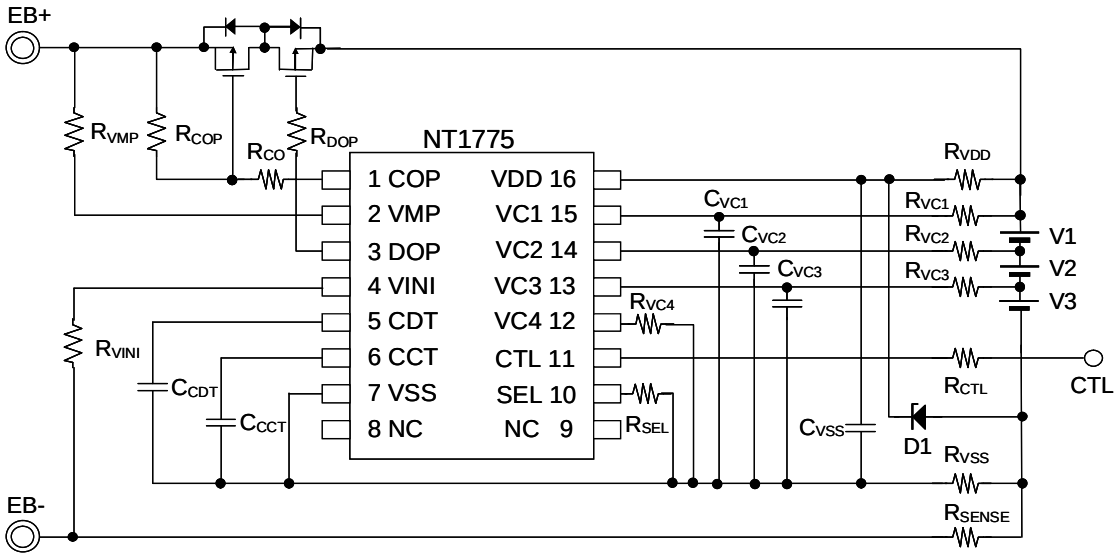


(2) Overcurrent Detection

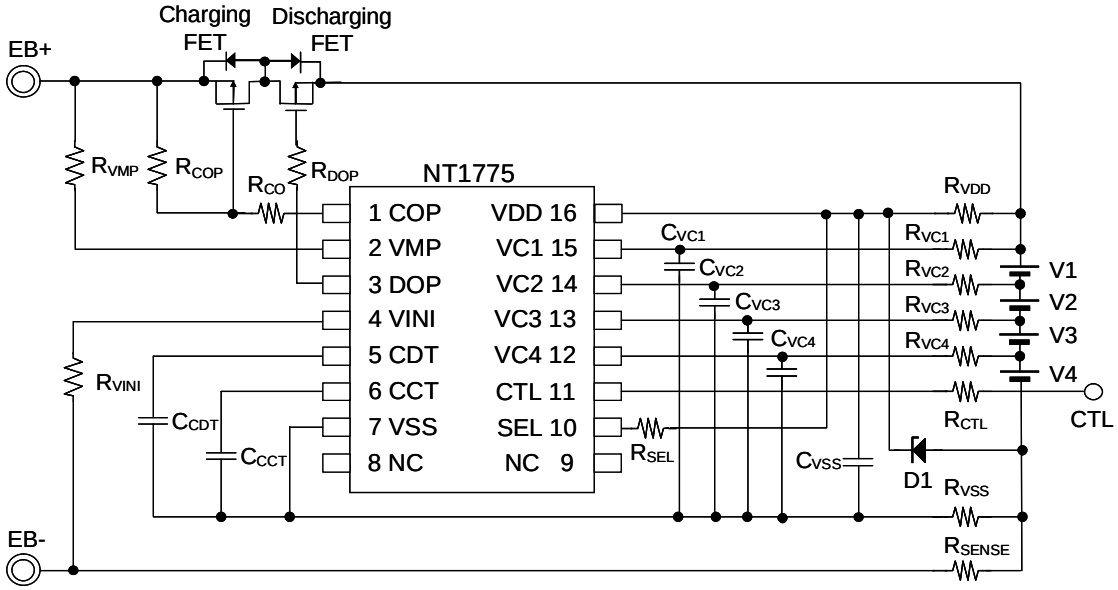


Application Circuit

1. 3-cell Application



2. 4-cell Application



Constant for external components

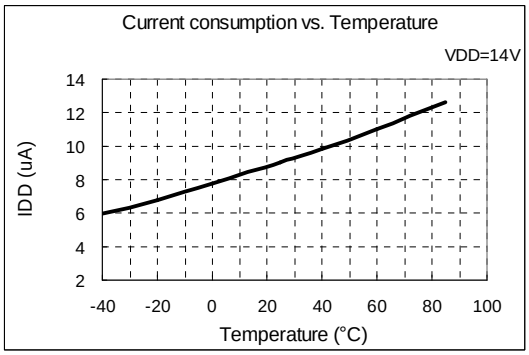
Symbol	Parts	Recommend	Min.	Max.
Charging FET	P channel MOSFET	----	----	----
Discharging FET	P channel MOSFET	----	----	----
R_{VDD}	Resistor	51Ω	4.7Ω	100Ω
R_{VC1}	Resistor	1KΩ	1KΩ	10KΩ
R_{VC2}	Resistor	1KΩ	1KΩ	10KΩ
R_{VC3}	Resistor	1KΩ	1KΩ	10KΩ
R_{VC4}	Resistor	1KΩ	1KΩ	10KΩ
R_{CO}	Resistor	5.1KΩ	2KΩ	10KΩ
R_{DOP}	Resistor	5.1KΩ	2KΩ	10KΩ
R_{COP}	Resistor	1MΩ	0.1MΩ	1.2MΩ
R_{VMP}	Resistor	100KΩ	51KΩ	120KΩ
R_{CTL}	Resistor	1KΩ	1KΩ	100KΩ
R_{VINI}	Resistor	1KΩ	1KΩ	100KΩ
R_{SEL}	Resistor	1KΩ	1KΩ	100KΩ
R_{SENSE}	Resistor	----	----	----
R_{VSS}	Resistor	0Ω	0Ω	51Ω
C_{VC1}	Capacitor	0.1μF	0.1μF	0.33μF
C_{VC2}	Capacitor	0.1μF	0.1μF	0.33μF
C_{VC3}	Capacitor	0.1μF	0.1μF	0.33μF
C_{VC4}	Capacitor	0.1μF	0.1μF	0.33μF
C_{CCT}	Capacitor	0.1μF	----	----
C_{CDT}	Capacitor	0.1μF	----	----
C_{VSS}	Capacitor	2.2μF	2.2μF	10μF
D1	ZENER	24V	----	----

1) If the threshold voltage of an FET is lower than 0.4V, the FET may not stop the charging current.
   If the charger voltage is higher than the withstanding voltage between the gate and source, the FET may be damaged.
2) For good noise immunity, C_{VC1}, C_{VC2}, C_{VC3}, C_{VC4} should be connected to ground.
3) For short-circuit protection, the R_{CO} should be placed for current limit.
4) Using an overspec R_{VC1}, R_{VC2}, R_{VC3}, R_{VC4}, may result in overcharge detection voltage and release voltage higher than the expectation.
   If R_{VC1} has a high resistance, the voltage between VDD and VSS may be higher than absolute maximum rating when a charger is connected reversely since the current flows from the charger to IC.

Caution: The application circuit above is for reference only. To determine the correct constants, evaluation of actual application is required.

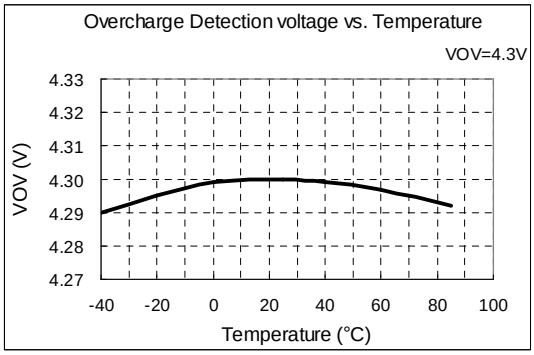
Characteristics (Typical Data)

1. Current consumption

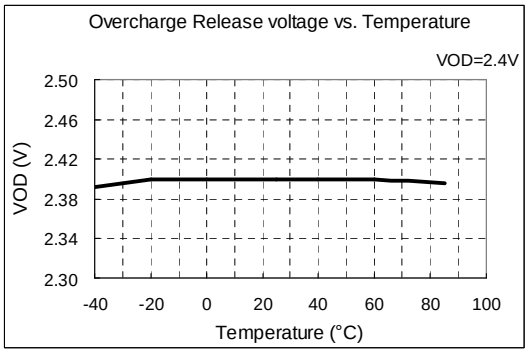


2. Detection Voltage

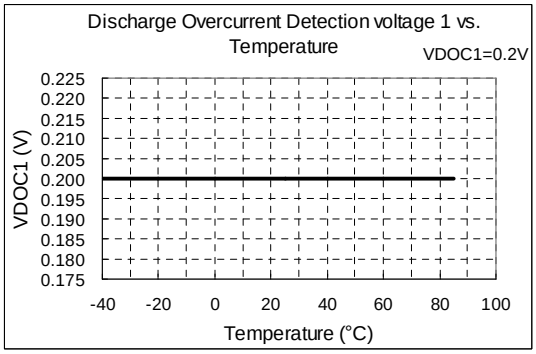
2.1 V_{OV} vs. Ta



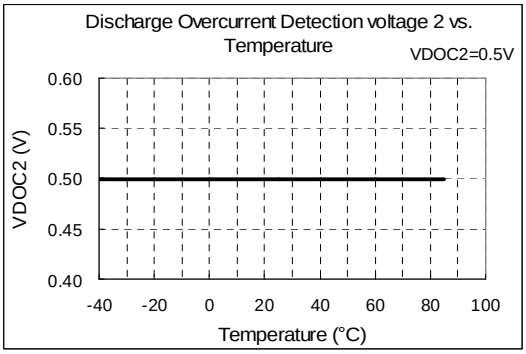
2.2 V_{OD} vs. Ta



2.3 V_{DOC1} vs. Ta

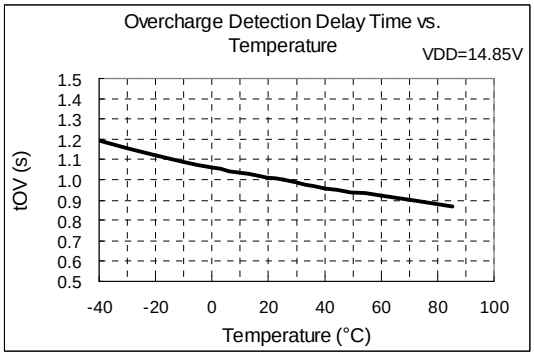


2.4 V_{DOC2} vs. Ta

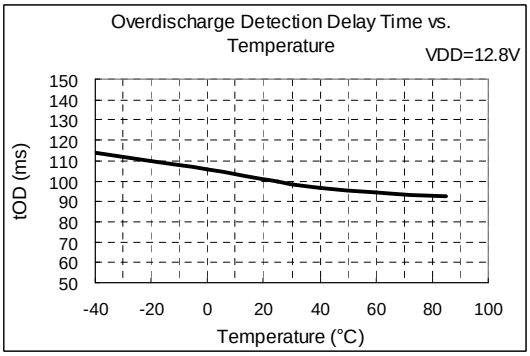


3. Detection Delay time

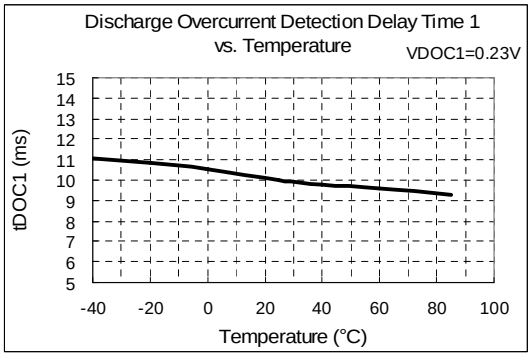
3.1 tOV vs. Ta



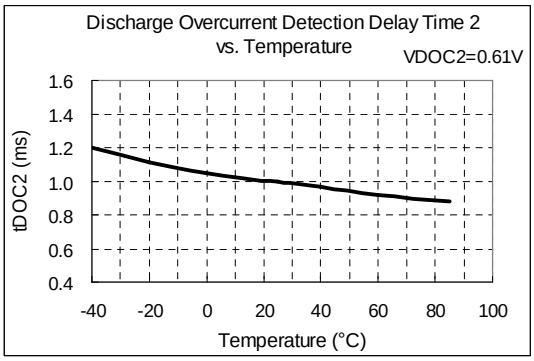
3.2 tOD vs. Ta



3.3 tDOC1 vs. Ta

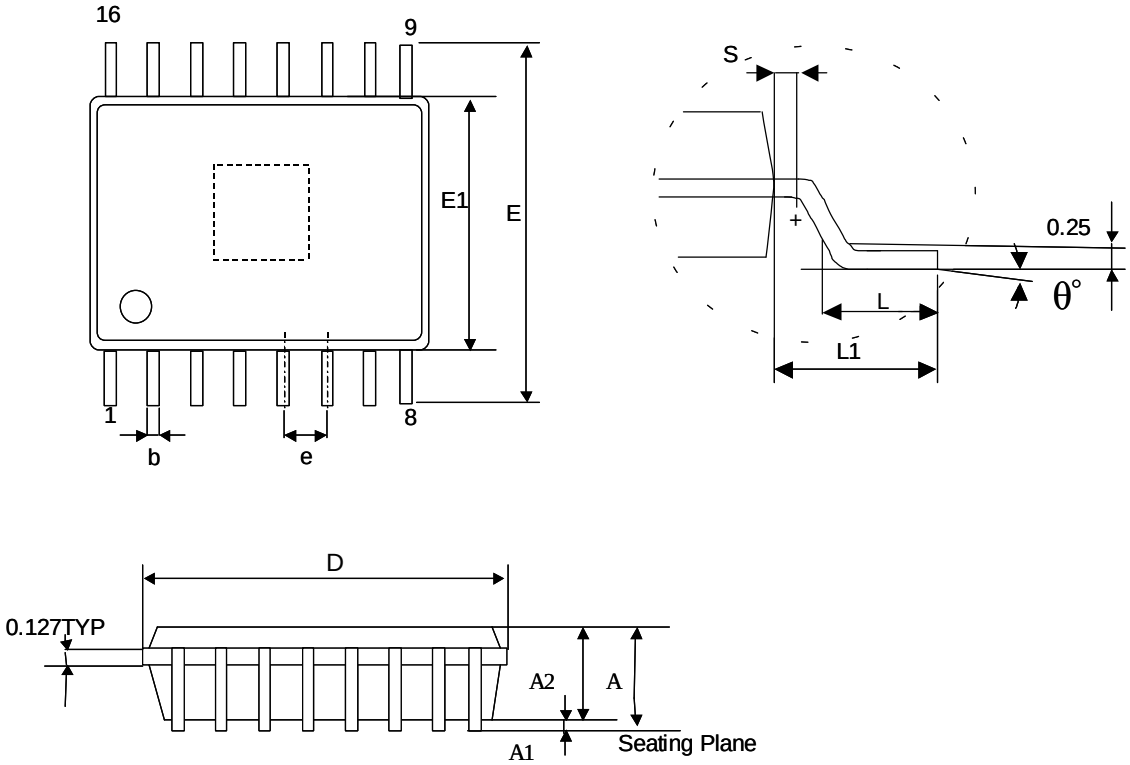


3.4 tDOC2 vs. Ta



Package Information

16-Pin TSSOP



SYMBOL	MIN.	NOM.	MAX.
A	—	—	1.20
A1	0.00	—	0.15
A2	0.80	1.00	1.05
b	0.19	0.22	0.30
D	4.9	5.0	5.1
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e	—	0.65BSC	—
L	0.45	0.60	0.75
L1	—	1.00	—
θ	0°	—	8°
θ 1	—	12REF	—

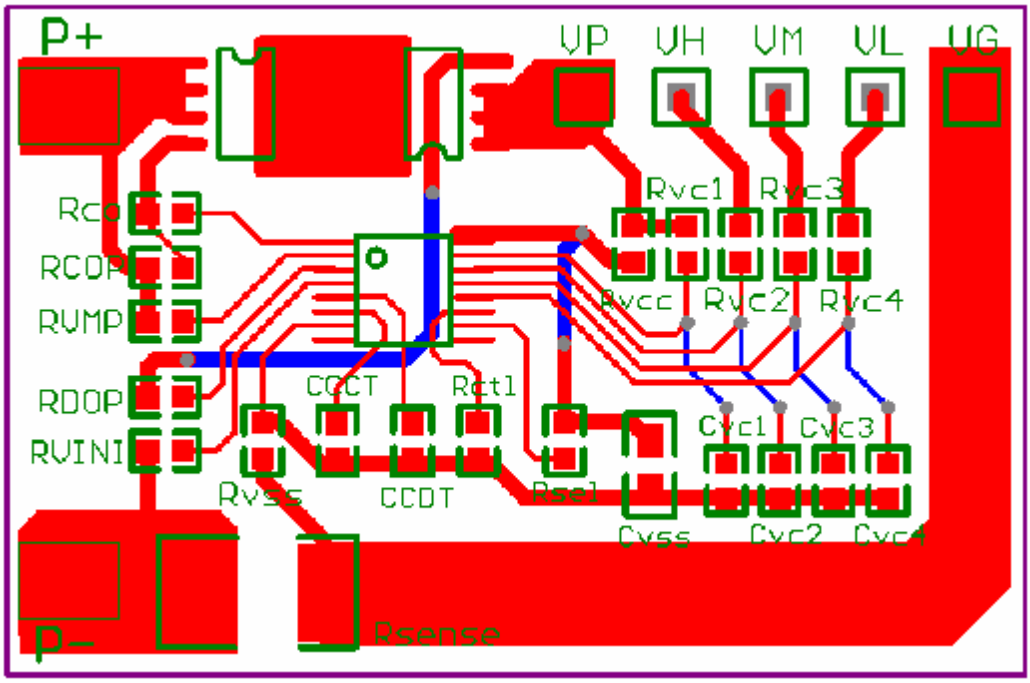
NOTES:1.All dimensions show in mm

2.Reference : JEDEC MO-153AB

3.TSSOP-16L-A

Layout Guide

For 4-cell application



Revision History

Version	Date	Revision	Page
3.08	2008/02/14	1) Add temperature coefficient	18~19
3.07	2008/02/01	1) Update the specification of short-circuit detection delay time	4
3.06	2007/11/16	1) Update the constant of R_{VDD} and R_{VMP} 2) Add layout guide	17 19
3.04	2007/7/16	1) Add some application note 2) Update the package information	17 18
3.03	2007/6/26	1) Update the Marking information	2